

TS11 Subsystem

User Guide

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TS11 Subsystem

User Guide

Prepared by Educational Services
of
Digital Equipment Corporation

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The TS11 Subsystem is a low price, medium performance, 9-track tape storage system featuring micro-processor controlled electronics for high data reliability and maintainability.

The TS11 fully integrated tape storage system is packaged with its associated interface and power supply in a standard 19 inch rack mountable frame. It can be configured in several cabinets to complement various DIGITAL computer systems. Reading and writing are performed at 45 inches per second and data is recorded at 1600 bits per inch (bit/in) phase encoded (PE). ANSI standard format recording allows data to be transferred easily between computer systems.

The TS11 Subsystem consists of a tape transport with an integrated formatter and a single hex size interface/controller module. This module, M7982, is designed for Unibus PDP-11 and VAX-11 processors. It plugs into any hex sized slot in a Unibus small peripheral controller (SPC), and it communicates with one tape transport.

SUBSYSTEM FEATURES

Performance

- 114 cm/sec (45 inches/sec) read/write speed
- 72,000 bytes per second transfer rate
- 380 cm/sec (150 inches/sec) rewind speed
- Bidirectional reading capability

Capacity

- 1600 bit/in phase encoded ANSI compatible recording
- 15.24 cm to 26.67 cm (6 inches to 10.5 inches) tape reel capacity

Reliability/Data Integrity

- Automatic error correction
- Read after write check
- In-line diagnostics that run continuously during drive standby mode
- Off-line self diagnostics
- Simple, rugged design

1.2 SUBSYSTEM OVERVIEW

Figure 1-1 shows the TS11 Subsystem block diagram. The Subsystem contains one transport, one TS11 interface module (M7982), and a serial bus interface cable.

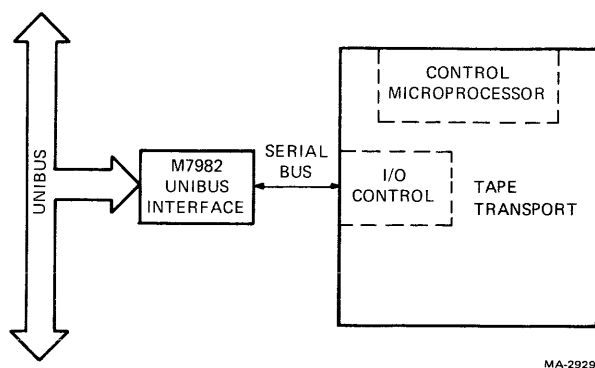


Figure 1-1 TS11 Subsystem Configuration

The M7982 interface plugs into the Unibus and receives parallel data in the packet protocol format. (Packet protocol is discussed in Chapter 5 of this manual.) A serial bus interface cable then connects the interface to the transport. Parity for the transport command and data information is maintained and checked in the serial data stream. This ensures that an accurate transfer has been made on the serial bus interface cable.

During data transfers, the transport resident formatter controls data fetching, formatting, and transmission. It also oversees the handling of error corrections. Single track read errors are corrected by the hardware automatically. The read after write feature verifies accurate recording of data on the tape.

Each vertical frame of the 9-track tape represents one character of eight bits plus a parity bit. Groups of characters are combined to form records that, under program control, can vary in length. Each record block is separated by a formatted interrecord gap (IRG) that has a minimum length of 0.5 inches.

The TS11 Subsystem features bidirectional tape reading. Writing occurs only while the tape is moving forward. Tape motion is controlled by a servo controlled capstan. Tape buffering between capstan and reels is accomplished by low inertia tension arms.

The tape drive can be controlled locally from the front control panel. All operational tape motion is controlled by two pushbutton switches.

Whenever the TS11 is in standby mode for more than 500 ms, an extensive set of drive resident diagnostics is executed to assure the continued operating integrity of the TS11. These diagnostics exercise the electronics to the fullest extent possible short of moving the tape or altering data and status register contents.

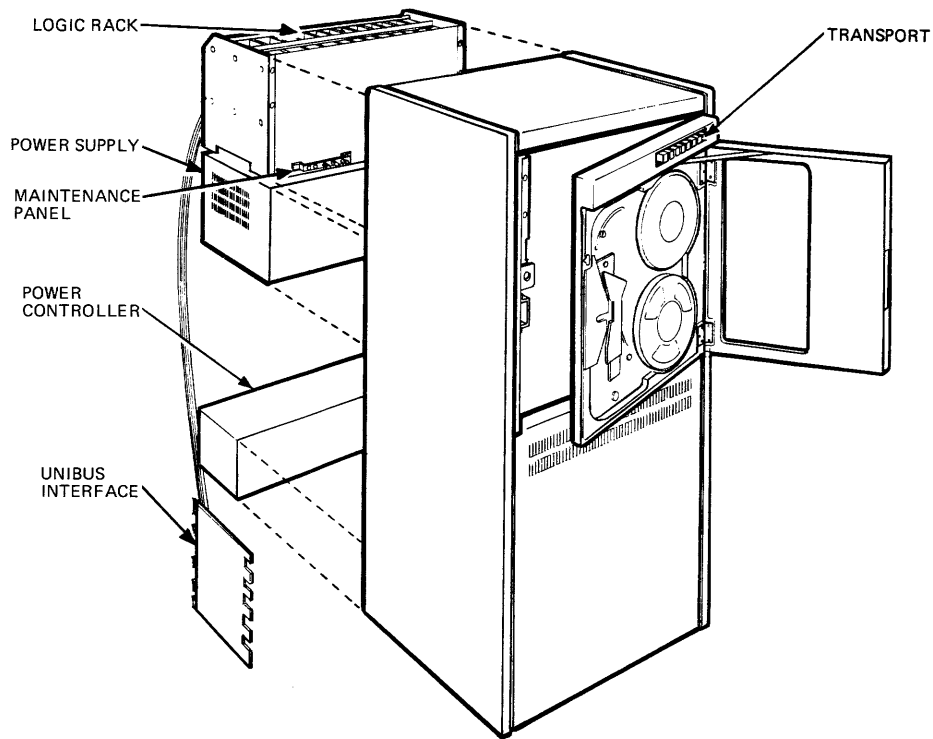
The TS11 microprocessor controls such things as capstan speed; it monitors read and write strobe times, sets read and write voltage threshold levels, and determines the length of interrecord gaps. This advanced control system provides further confidence in the operating integrity of the TS11.

1.3 PHYSICAL DESCRIPTION

Figure 1-2 shows the TS11 Subsystem major assemblies.

1.3.1 Unibus Interface

The Unibus interface is a standard PDP-11 hex height, multilayer two sided module (M7982 module designation). It can be placed in any small peripheral controller (SPC) slot that is wired for all Unibus signals and accepts hex height modules. Also, it can plug into DD-11 series SPC backplanes in BA11 series expander boxes. This module links the transport with the Unibus via a serial bus interface cable.



MA-2967

Figure 1-2 TS11 Subsystem Major Assemblies

NOTE

The nonprocessor grant (NPG) jumper must be removed when the M7982 is installed.

1.3.2 Transport

The tape transport subsystem (Figures 1-2 and 1-3) is comprised of the following major assemblies.

- Main deck plate
- Reel servo
- Capstan servo
- Head assembly and read preamplifiers
- Tape transport control and operator control logic
- Power supply

Main Deck Plate – The main deck is die cast aluminum. It provides a single co-planar set of mounting surfaces. These machined surfaces become a single reference plane on which all tape path determining parts are mounted. (Reference Figures 1-2 and 1-3.)

The casting, and hence the drive, is mounted to a cabinet rack by two hinge blocks. It swings out (hinged on the right side) to allow servicing. Also, for servicing, several reference pads are provided to check hub and reel alignment. The door, mounted to the same hinge area, can also be opened if the drive is swung outward.

Reel Servo – The reel servo consists of the supply reel servo motor and snap lock hub, take-up reel servo motor and take-up reel, G158 reel motor control module, and tension arm assemblies (reference Figures 1-3 and 1-4). All of these components mount directly to the main deck assembly.

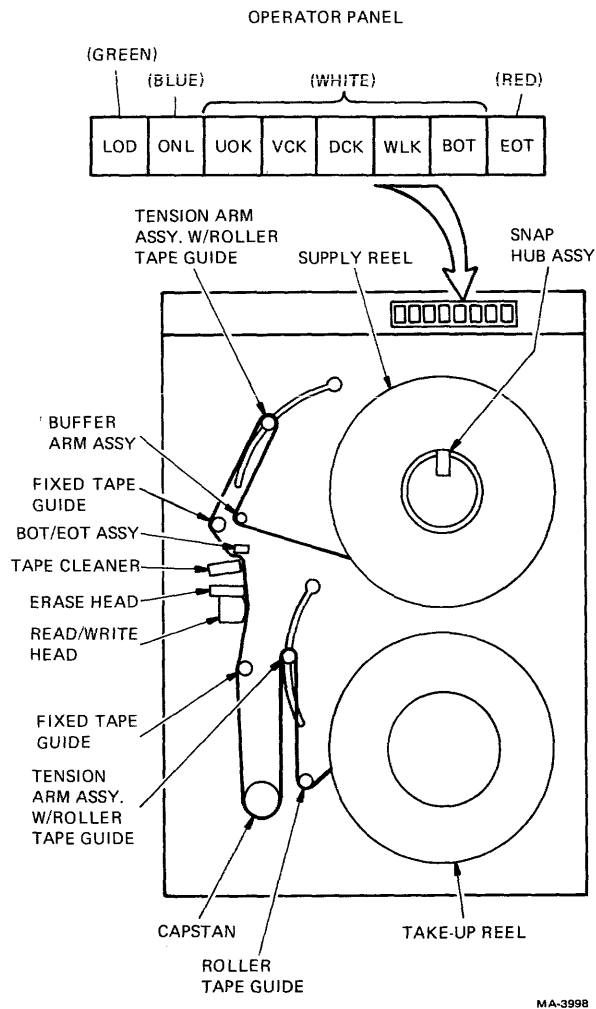


Figure 1-3 Transport Assemblies (Front View)

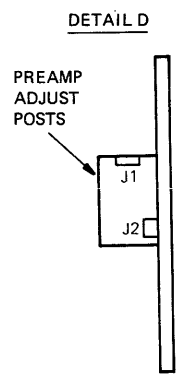
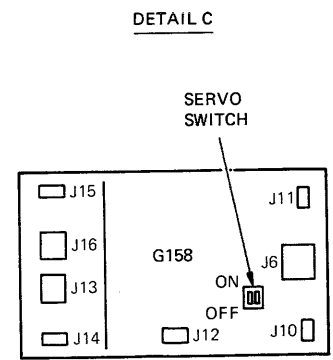
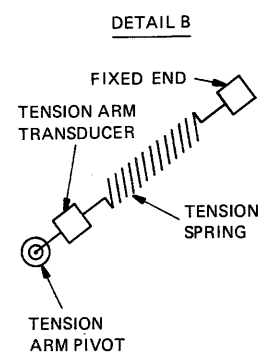
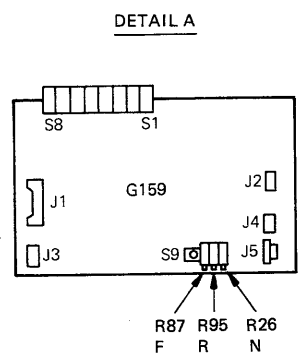
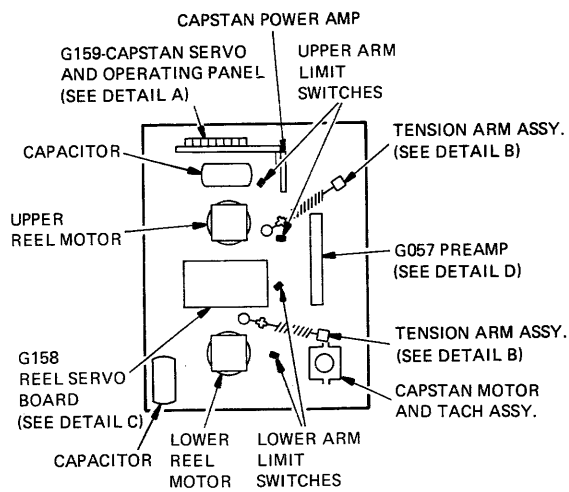
The tension arms control tape tension and allow rapid tape start and stops without damage to the tape or servo motors. Tension arms also sense tape motion in order to drive the reel servo motors. The G158 module receives these signals and controls the speed and direction of both servo motors.

Capstan Servo – The capstan servo system consists of the capstan motor/tachometer assembly and the G159 capstan servo module (reference Figures 1-3 and 1-4). The capstan motor assembly moves the tape across the read/write head. The G159 module sets the direction and drives the motor while the optical tachometer senses the tape speed. The optical tachometer then loops the information back to the G159 module, which in turn drives the capstan motor to the correct speed.

Head Assembly – The head assembly consists of a precision head mounting plate, read/write head, head tape guides, tape cleaner, erase head, and an EOT/BOT sensor (reference Figure 1-3). The head mounting plate provides a precision mounting surface for the head, cleaner, and guides.

The G057 module (Read Preamplifiers) is contained in a shielded enclosure and mounted to the rear of the deck casting.

Operator Controls – The transport (reference Figure 1-3) incorporates three lighted operator push buttons (colored) and five indicators (white). Chapter 4 details the operation of these controls.



MA-4007

Figure 1-4 Transport Assemblies (Rear View)

These controls perform a dual function: operating and diagnostic control. Microdiagnostic errors will be displayed in either mode. A switch on the printed circuit board backplane selects the mode.

Power Supply – All transport voltages are supplied by the TS11 power supply. The supply operates at 50 or 60 Hz \pm 1 Hz with no changes required. For 120 V or 240 V operation, only the ac input box and line cord need to be changed. A TS11K-AA kit converts a 240 V unit to 120 V and a TS11K-AB kit converts a 120 V unit to 240 V. The power system is modularized for easy maintenance and uses standard parts for increased reliability.

1.4 SYSTEM FUNCTIONAL DESCRIPTION

The functions listed in Table 1-1 make up the TS11 Subsystem command set. These commands use device registers to operate the transport and to transfer data. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data). Detailed descriptions of the commands are provided in Chapter 5 of this manual.

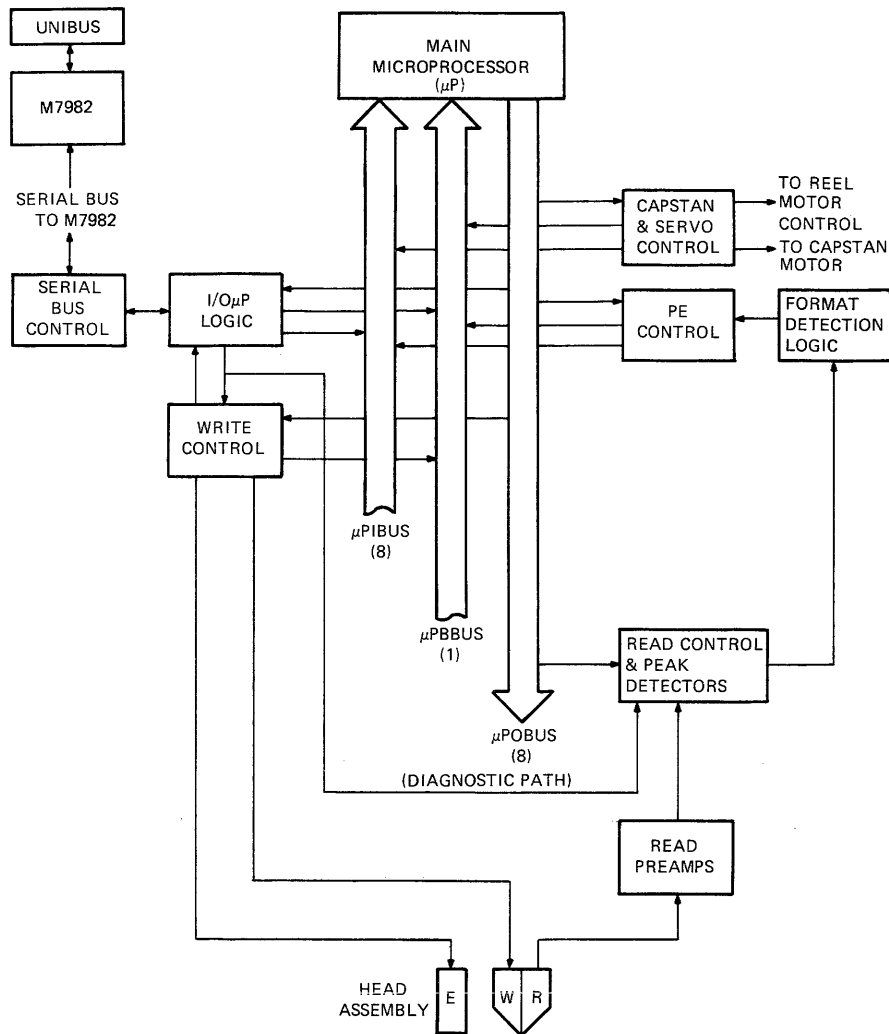
Table 1-1 TS11 Assigned Command Modes

Command Name	Mode Name
Get Status	Get status
Read	Read next (forward) Read previous (reverse) Reread previous (space reverse, read forward) Reread next (space forward, read reverse)
Write Characteristics	Load message buffer address and set device characteristics
Write	Write data Write data retry (space reverse, erase, write data)
Position	Space records forward Space records reverse Skip tape marks forward Skip tape marks reverse Rewind
Format	Write tape mark Erase Write tape mark retry (space reverse, erase, write tape mark)
Control	Message buffer release Rewind and unload Clean tape
Initialize	Drive initialize

Figure 1-5 is a simplified block diagram of the TS11 Subsystem. The transport is under the complete control of the microprocessor and related microcode. Two TS11 Subsystem registers (TSBA and TSSR) are presented to the Unibus and communication between the CPU and the transport is via packet protocol (controlled by the microcode).

The TS11 (M7982) has eight registers which occupy only two Unibus word locations: a Unibus data buffer (TSDB), a Unibus address register (TSBA), and a status register (TSSR). The five additional registers elsewhere in PDP-11 memory provide status information.

The TSDB is an 18-bit register that is parallel loaded from the Unibus or serially loaded from the transport. A 16-bit portion of this register is used as a word buffer register to the M7982 when the M7982 is the bus slave (for beginning an operation). The same word buffer register is also used by the transport [for data during nonprocessor request (NPR) transfers] when the M7982 is the bus master. The TSDB can be loaded when the M7982 is the bus slave by three different transfers from a bus master. Two transfers are for maintenance purposes (byte transfer; DATOB at high/low byte). The third transfer is for normal (word) operation (DATO). This register is write only and is not cleared at power on, subsystem initialize, or bus initialize. It cannot be loaded without the complete transport unit connected (to supply a serial bus synchronous clock). The M7982 responds with SSSYN (system synchronized) every time the TSDB is accessed.



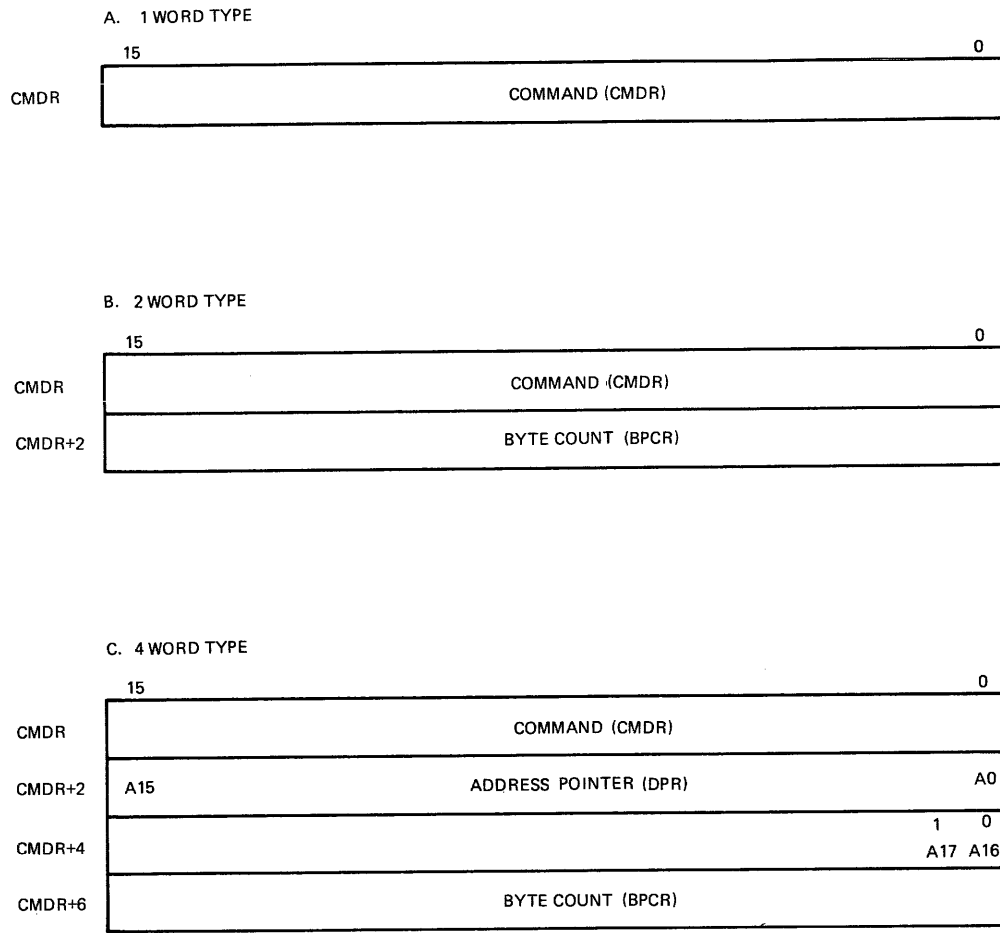
MA-2933

Figure 1-5 TS11 Simplified Block Diagram

Commands are not written to the drive's Unibus registers. Instead, command pointers, which point to a command packet somewhere in memory space, are written to the TSDB register. The command pointer is used in the TS11 Subsystem to retrieve words in memory called the command packet. The words in the command packet instruct the transport as to the function to be performed. These words contain any function parameters such as bus address, byte count, record count, and modifier flags.

The TSBA is an 18-bit register that is parallel loaded from the TSDB every time the TSDB is loaded as Unibus slave. TSDB bits 15-2 load into TSBA bits 15-2; TSDB bits 1 and 0 load into TSBA bits 17 and 16; and zeros are loaded into TSBA bits 1 and 0. TSBA bits 17 and 16 are displayed in TSSR bits 9 and 8 respectively. The register can be instructed by the transport to increment or decrement by two for nonprocessor request (NPR) word transfers, or by one for NPR byte transfers. The TSBA register has two major purposes.

1. The TSBA can be used as a command pointer to the remote transport device registers (command and message buffers). These are located somewhere in the Unibus address space. The contents, loaded into the TSDB when the M7982 is the bus slave, is considered the command pointer. In this mode, the M7982 receives data (initiated by the transport) at this



MA-3863

Figure 1-6 Command Packets

command pointer address and sends the command packet (data) to the drive unit for storage and/or execution.

2. The TSBA can be used as a data pointer, pointing to data buffer areas located somewhere in the Unibus address space. In this mode, the transport serially loads the TSDB with the data buffer address and transfers the contents of TSDB (0-17) into TSBA. The contents are then used to point to data buffer areas [while the M7982 transfers data by the NPRs (initiated by the transport)] and to message packets where the TSBA is left with the highest message buffer address + 2.

The TSSR is a 16-bit register that can be updated only from the transport or M7982 internal logic. It cannot be modified from the Unibus except for SPE, UPE, RMR, NXM, and SSR bits that are cleared when the TSDB is written by the host CPU. Here system status can be observed.

Before the TS11 Subsystem can begin a function, a command packet must be assembled in the system memory. In every case the packet must be comprised of four words, even though not every command requires all four words. The packet may be thought of as three remote device registers (Figure 1-6).

1. Command Register (CMDR)

2. Data Pointer (DPR) which is comprised of two word locations:

Low order address word (A15:00) CMDR+2
High order address word (A17:16) CMDR+4
in bits 1 and 0

3. Positive Byte Count Register (BPCR)

Data operations (DPR required) CMDR+6
Nondata operations (no DPR required) CMDR+2

Message packets are issued by the transport and deposited in the host CPU memory space. These message packets contain complete device status information. Subsystem operation requires a message buffer address on a set characteristics command. This command must be the first command issued to the subsystem. Otherwise, all tape motion commands will be rejected.

The command pointer must be an address on a modulo-4 boundary (that is, beginning at 0, 4, 10, 14, etc.), because only the high order 16-bits can be specified by the command pointer.

The DPR is eventually loaded into TSBA to be used as the Unibus address for NPR data transfers. The BPCR is used to indicate the number of bytes (8-bits of data per byte) to be moved to or from the transport during a data transfer. It is also used to specify the number of records in a space record command or the number of files in a skip file command. The CMDR specifies the function to be executed by the transport.

Figure 1-5 is a simplified block diagram of the TS11 Subsystem. If a read forward operation is commanded, the following occurs. The capstan interface logic directs the capstan servo logic to supply motor current to the capstan servo. This moves the tape forward. When the tape is up to speed, the transport read logic is enabled and receives data from the read heads. The read data output of the read heads (RD0-RD7, RDP) is checked for vertical parity errors. If any such errors are detected, the transport error logic is notified to take appropriate corrective action.

Read data from the formatter is then sent to the main microprocessor via the microprocessor in bus (μ PIBUS). Under microprocessor control, read data is then sent to the I/O control and sequencing logic via out bus (μ POBus). From here, the I/O microprocessor transfers read data to the serial bus control logic via the I/O out bus (I/O OBus), where the data is gated serially to the M7982 interface. A serial to parallel conversion occurs and the data word is parallel transferred to memory via the Unibus on the M7982.

If a write operation is commanded and the request is granted, the following occurs. The capstan servo logic supplies motor current to the capstan, moving the tape forward. The first data character is placed on the Unibus and enters the M7982 when requested by the microprocessor. Subsequent transfers occur and fill up the silo in the I/O microprocessor, before writing on tape occurs. When the tape is up to speed, transferring data characters begins. As data characters are written on tape, new characters are transferred to the silo. This occurs until all data is transferred from memory to silo, and finally, silo to tape. The Preamble is loaded into the silo before write data. Postamble is loaded in after. All data transfers (serial transfers) are under the control of the I/O microprocessor. The data is sent via the serial bus cable to the serial bus control logic. The I/O bus then transfers data to the write control logic and on to the write heads. The main microprocessor checks the data for write errors by doing a read after write.

Detailed operation of the TS11 is provided in Chapter 6 of the *TS11 Subsystem Technical Manual*.

1.5 UNIT SPECIFICATIONS

Table 1-2 lists the operational, environmental, mechanical, and electrical specifications for the TS11 Subsystem.

Table 1-2 TS11 Subsystem Specifications

Category	Specifications
Main Specifications	
Storage medium	12.7 mm (0.5 in) wide magnetic tape (industry compatible)
Data transfer rate	72,000 characters per second, maximum
Transports per controller	1
Data Organization	
Number of tracks	9
Recording density	64 rows/mm (1600 bpi)
Interrecord gap	12.7 mm (0.5 in) minimum
Recording method	PE mode at 64 rows/mm (1600 bpi); conforms with ANSI DOC. X3.39-1973
Tape Motion	
Speed, forward and reverse	114 cm/sec (45 in/sec)
Rewind speed	380 cm/sec (150 in/sec) 3 minute average for 10.5 inch reel
Tape transport	Direct drive ac reel motors, servo controlled; capstan has biphas tachometer outputs tension arm tape buffering with constant tension
Start distance	4.57 mm \pm 0.5 mm (0.180 in \pm 0.050 in)
Stop distance	4.11 mm \pm 1.1 mm (0.162 in \pm 0.050 in)
Start time	8 ms \pm 1 ms
Stop time	8 ms + 1 ms -2 ms
Tape Characteristics	
Width	12.7 mm (0.5 in)
Length	732 m (2400 ft) maximum
Type	Mylar base, iron-oxide coated (ANSI standard)
Thickness	0.038 mm (1.5 mils)
Tension	227 g (8.0 oz)
Reel diameter	26.7 cm (10.5 in)
Reel hub	9.37 cm (3.69 in) diameter (industry standard)
Mechanical	
Tape transport mounting	Mounts on slides in standard 48.3 cm (19 in) cabinet
Transport dimensions in rackmount option	
Depth	76 cm (30 in)
Width	48 cm (19 in)
Height	66 cm (26 in)
Weight	68 kg (150 lb)
Electrical	
Frequency	50 Hz \pm 1 Hz or 60 Hz \pm 1 Hz
Voltage	90-128 Vac or 184-256 Vac single phase

Table 1-2 TS11 Subsystem Specifications (Cont)

Category	Specifications
Power	400 W (standby); 1200 W maximum (start/stop)
Input current (Transport)	10 A maximum @ 90-128 Vac; 5 A maximum @ 184-256 Vac
Input current (M7982 Interface)	3.5 A maximum @ 5 Vdc
Environment	
Operating temperature	15° to 32° C (60° to 90° F)
Relative humidity	20% to 80%, with maximum wet bulb 25° C (77° F) and minimum dew point 2° C (36° F)
Maximum altitude	2438 m (8000 ft)
Other	
BOT, EOT detection	Photoelectric sensing of reflective strip (industry standard)
Skew control	Deskewing electronics in the tape transport correct static skew
Write protection	Write protect ring sensing on the tape transport
Magnetic heads	Nine track, dual gap read after write (full-width erase)

1.6 APPLICABLE DOCUMENTS

The documents listed in Table 1-3 are applicable to the TS11 system and are available through the local DIGITAL Sales and Service Office or the Accessories and Supplies Group. See Section 3.3.4 for details.

1.7 AVAILABLE OPTIONS

Table 1-4 lists the options available for the TS11 Subsystem.

Table 1-3 Applicable Documents

Title	Number	Description
TS11 Subsystem User Guide	EK-0TS11-UG	Contains functional overview, installation, operating, and programming information.
TS11 Subsystem Technical Manual	EK-0TS11-TM	Combines the user guide with theory of operation and maintenance information.
TS11 Subsystem Pocket Service Guide	EK-0TS11-PS	Provides a quick reference to maintenance procedures for the trained service person.
TS11 Subsystem Illustrated Parts Breakdown		Provides a listing and illustration of replaceable parts.
872 Power Controller	EK-00872-IP	
861 Power Controller	EK-00861-IP	
TS11 A	EK-TS11A-IP	
TS11 B	EK-TS11B-IP	
TS11 C	EK-TS11C-IP	
TS11 D	EK-TS11D-IP	
PDP-11 Processor and Systems Manual*		A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 system.
PDP-11 Processor Handbook**		A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.

* Applicable manuals accompany the system at the time of installation. The document number depends on the specific PDP-11 family processor.

** Use the processor handbook unique to the actual CPU.

Table 1-4 Available Options

Option	Description
TS11-AA	Rackmount with M7982 120 Vac, 50/60 Hz
TS11-AB	Rackmount with M7982 240 Vac, 50/60 Hz
TS11-BA	TS11-AA in H9602 corporate cabinet
TS11-BB	TS11-AB in H9602 corporate cabinet
TS11-CA	TS11-AA in H9646 cabinet
TS11-CB	TS11-AB in H9646 cabinet
TS11-DA	TS11-AA in H960 tall cabinet
TS11-DB	TS11-AB in H960 tall cabinet
TS11K-AA	TS11 240 Vac to 120 Vac conversion kit
TS11K-AB	TS11 120 Vac to 240 Vac conversion kit

CHAPTER 2 INSTALLATION

2.1 SITE PLANNING AND CONSIDERATIONS

Before installing the TS11 Subsystem, careful site planning is necessary to satisfy physical and electrical requirements. These aspects of site preparation are discussed in the following paragraphs.

2.1.1 Space Requirements

The transport is available as a rackmount option or as an H960, H9602, H9646 cabinet. Figures 2-1, 2-2, and 2-3 respectively illustrate the space and service clearance required for each cabinet.

The TS11 interface requires a single slot in an SPC backplane or DD-11 series SPC backplane in a BA11 series expander box.

The transport must be located close enough to the M7982 mounting slot to accommodate an interconnecting cable of 7.4 m (25 feet).

2.1.2 Power Requirements

Both the $60 \pm 1\text{Hz}$ and $50 \pm 1\text{Hz}$ transports operate from 90-128 Vac or 184-256 Vac power sources. Operating input power is approximately 400 W nominal (standby), with an operating peak of approximately 1200 W. Maximum operating current in the low voltage range is 10.0 A rms maximum; in the high voltage range it is 5.0 A rms.

Table 2-1 provides a list of receptacles that accept the various voltages. The appropriate circuit breakers are also necessary.

The TS11 (M7982) typically draws 2.0 A, with a maximum of 3.5 A, calculated at +5 Vdc. No other voltage is required. A hex height SPC module is allowed to draw a maximum of 6 A at +5 Vdc (1 A maximum per module section) from an SPC slot. Do not exceed the power available to an SPC slot, DD-11 backplane, or expander box. Also, maximum usable SPC power is not always available in expander boxes. Be sure sufficient power is available.

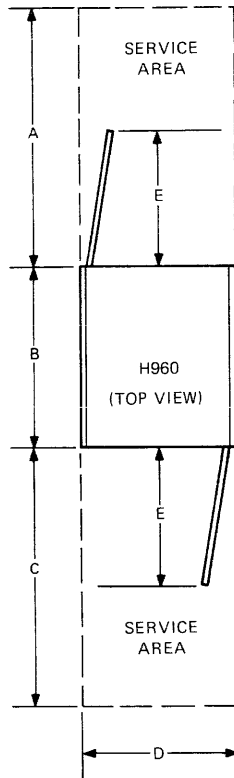
Digital Equipment Corporation must be notified of available input power well in advance of shipment, so that the correct TS11 Subsystem can be shipped.

2.1.3 Floor Loading

Floor loading data is listed in Table 2-2.

2.1.4 Installation Constraints

The route that the equipment will travel from the receiving area to the installation site should be studied in advance to ensure problem free delivery. Among the factors to be considered are the height and location of loading doors, the size, capacity, and availability of elevators, the number and size of aisles and doors en route, and any restrictions, such as bends or obstructions, in the hallways. Any constraints should be reported to Digital Equipment Corporation as soon as possible so that requirements of the individual installation site can be considered when the unit is packed for shipment.



NOTES:

1. REAR DOORS MAY BE LH OR RH. ALLOW SPACE FOR EITHER CASE.
2. CABINET IS 182.28cm. (71 7/16in.) HIGH (FLOOR LINE TO CABINET TOP).
3. IF THIS IS A STAND-ALONE OR THE END CABINET (ie., NO ADDITIONAL CABINET BOLTED TO THIS SIDE) THE END PANEL MUST BE REMOVED BEFORE THE TRANSPORT ASSEMBLY CAN BE SWUNG OPEN.

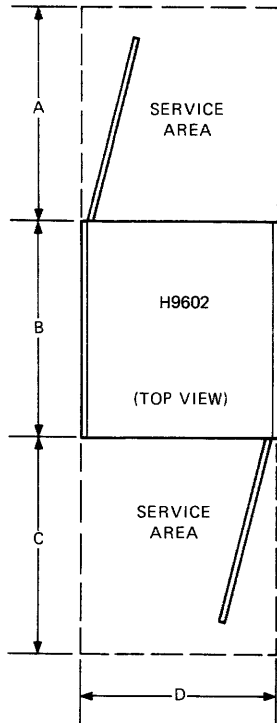
MA-3553

DIMENSIONS	A	B	C	D	E
INCHES	36	29	36	22	19.5
CENTIMETERS	91.5	73.7	91.5	55.9	49.5

Figure 2-1 Space and Service Clearance, H960 Cabinet and Rackmount (Top View)

Table 2-1 TS11 Power Plugs and Receptacles

Rackmount	Plug	Receptacle
120 V NEMA	5-15P	5-15R
120 V DIGITAL	90-08938	12-05351
240 V NEMA	6-15P	6-15R
240 V DIGITAL	90-08853	12-11204
Digital Standard Cabinets (H960, H9602, H9646)	Plug	Receptacle
120 V NEMA	L5-30P	L5-30R
120 V DIGITAL	12-11193	12-11194
240 V NEMA	L6-20P	L6-20R
240 V DIGITAL	12-11192	12-11191



NOTES:

1. REAR DOORS MAY BE LH OR RH, ALLOW SPACE FOR EITHER CASE.
2. TRANSPORT ASSEMBLY SWINGS OPEN RH ONLY. LOWER FRONT CABINET DOOR SNAPS ON AND OFF, IT DOES NOT SWING.
3. 127 cm. (50 in) OR 152 cm. (60 in.) HIGH DEPENDING ON MODEL (FLOOR LINE TO CABINET TOP).

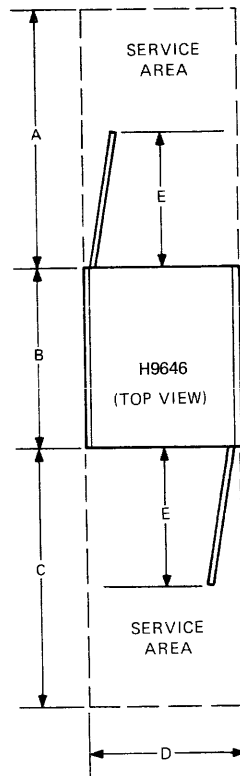
MA-3554

DIMENSIONS	A	B	C	D
INCHES	30	30	30	27.5
CENTIMETERS	76.2	76.2	76.2	69.9

Figure 2-2 Space and Service Clearance, H9602 Cabinet (Top View)

Table 2-2 Floor Loading

TS11 Option	Weight
TS11-AA/AB Rackmount (TS11 in mounting frame)	68 kg (150 lbs)
TS11-BA/BB Rackmount in H9602	231 kg (506 lbs)
TS11-CA/CB Rackmount in H9646	188 kg (415 lbs)
TS11-DA/DB Rackmount in H960	230 kg (504 lbs)



DIMENSIONS	A	B	C	D	E
INCHES	36	30	36	22	19.5
CENTIMETERS	91.5	76.2	91.5	55.9	49.5

NOTES:

1. CABINET IS 152.3cm (60 IN.) HIGH (FLOOR LINE TO CABINET TOP).

MA-3553A

Figure 2-3 Space and Service Clearance,
H9646 Cabinet (Top View)

The TS11 Subsystem should be located in an area free of excessive dust and dirt or corrosive fumes and vapors. Equipment should be placed so that cabinet fan inlets and air outlets are not obstructed in any way.

If the system you are installing is housed in an H9602 cabinet, the following precautions should be understood before installation.

1. Observe the caution symbols on the cabinet containers.
2. These cabinets arrive without shipping skids. A fork lift is not necessary, but one can be used if it lifts from the side of the cabinet.
3. When moving the cabinets, push them only on the side indicated by the caution symbols. The casters are locked to facilitate movement in the direction indicated.
4. Handle the cabinets carefully to avoid excessive shock.

CAUTION

Exercise special care when moving cabinets up or down ramps; they may become unstable when tilted more than 10 degrees.

2.1.5 Fire and Safety Precautions

The TS11 Subsystem does not present unusual or additional fire or safety hazards to an existing computer system. However, wiring should be carefully checked, to ensure that its capacity is adequate for the added load and for any contemplated expansion.

2.1.6 Temperature

The environmental operating temperature of the TS11 Subsystem may range from 15° to 32° C (59° to 90° F); the maximum gradient is 17° C per hour.

2.1.7 Relative Humidity

Humidity control is very important in a data storage system environment. Static electricity, which varies with humidity, can cause errors in any CPU with memory. The TS11 Subsystem operates efficiently in a relative humidity range of 20 to 80 percent with a maximum wet bulb temperature of 25° C (77° F) and a minimum dew point of 2° C (36° F).

2.1.8 Heat Dissipation

Heat dissipation of the transport is 900 Btu/hr nominal and 3800 Btu/hr maximum. The approximate cooling requirements for the system can be determined by performing the following calculations. Add the above figure to the maximum heat dissipation for the other system components. Then adjust the results to compensate for such factors as the number of personnel, heat radiation from adjoining areas, sun exposure through windows, system efficiency, etc. A safety margin at least 25 percent above the estimated cooling requirements is suggested.

2.1.9 Acoustics

While most computer sites require some degree of acoustic treatment the TS11 Subsystem should not contribute unduly to the overall acoustic problem. However, the acoustic materials at the site should not produce or harbor dust.

2.1.10 Altitude

Computer systems may encounter heat dissipation problems at high altitudes. At altitudes over 610 m (2000 ft), the maximum allowable operating temperature is reduced by a factor of 1.8° C for each 1000 m (1° F for each 1000 ft). The maximum altitude specified for the transport is 2438 m (8000 ft). Therefore, its maximum allowable operating temperature at 2438 m (8000 ft) would be reduced to 27.60° C (81.7° F).

2.1.11 Radiated Emissions

Radiation sources, such as FM or radar transmitters, in close proximity to the computer system may affect the operation of the processor and some peripheral equipment. The effects of these emissions can be minimized by the following actions.

1. Ground window screens and other large metal surfaces.
2. Shield interconnecting cables with a grounded shield.
3. Provide additional grounding to the system cabinets and chassis.

In environments subject to extreme radiation, the system may require a grounded cage.

2.1.12 Required Tools

In addition to the standard DEC Tool Kit (PN 29-18303), a spirit level is also required for unpacking and installation.

2.2 UNPACKING

The TS11 Subsystem may be shipped in four variations: as a rackmount version, or three cabinet styles (H960, H9602, or H9646). Unpacking and installation procedures vary with the choice of cabinets.

No matter which variation is chosen for the transport, the device is shipped with all interconnecting cables installed. The M7982 Unibus interface module is delivered in a separate package.

When packaged for shipment, the transport in its cabinet weighs up to 230 kg (500 lb). Although the package is excessively heavy and bulky for single-person handling, it does not require the use of a forklift or similar equipment to move or lift it.

CAUTION

When moving or lifting the transport, always grasp the frame structure. Do not hold any part of the top or side covers.

2.2.1 Rackmount Option

Unpack the rackmount option by performing the following actions.

1. Remove the outer shipping container.

NOTE

The container may be heavy corrugated cardboard or plywood. In either case, remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from the perimeter.

2. Remove the polyethylene cover from the transport. The transport is now ready to be mounted in its cabinet.

CAUTION

The TS11 AA/AB option weighs 68 kg (150 lbs). A minimum of two people are needed to move the transport to its mounting place.

2.2.2 H960 Cabinet Unpacking

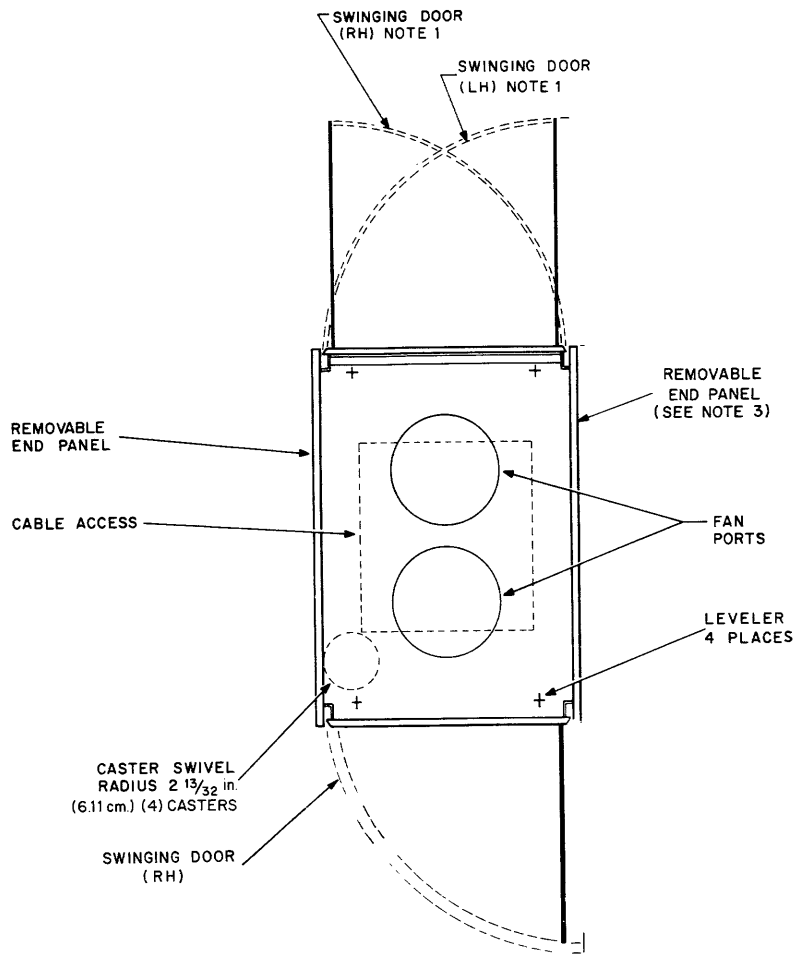
Unpack the H960 cabinet by performing the following actions.

1. Remove the outer shipping container.

NOTE

The container may be heavy corrugated cardboard or plywood. In either case, remove any fasteners and cleats securing the container to the skid. If applicable, remove the wood framing and supports from the cabinet perimeter.

2. Remove the polyethylene cover from the cabinet.



- NOTE:
1. REAR DOORS MAY BE LH OR RH. ALLOW SPACE FOR EITHER CASE.
 2. IF THIS IS A STAND-ALONE OR THE END CABINET (i.e., NO ADDITIONAL CABINET BOLTED TO THIS SIDE) THE END PANEL MUST BE REMOVED BEFORE THE TRANSPORT ASSEMBLY CAN BE SWUNG OPEN.

MA-3555

Figure 2-4 H960 Cabinet Installation

3. Unbolt the cabinet(s) from the shipping skid. Remove the bolts located on the lower supporting side rails; they are exposed by opening the access door(s).
4. Raise the leveling feet above the level of the roll around casters. Refer to Figure 2-4.
5. Use wood blocks and planks to form a ramp from the skid to the floor. Carefully roll the cabinet onto the floor.
6. Roll the system to the proper location for installation.

2.2.3 H9602 Cabinet Unpacking

Unpack the H9602 cabinet by performing the following actions.

1. Unbolt the bottom protector from the crate at the front, back, and sides. Remove the protector.
2. Unbolt and remove the front panel of the crate.

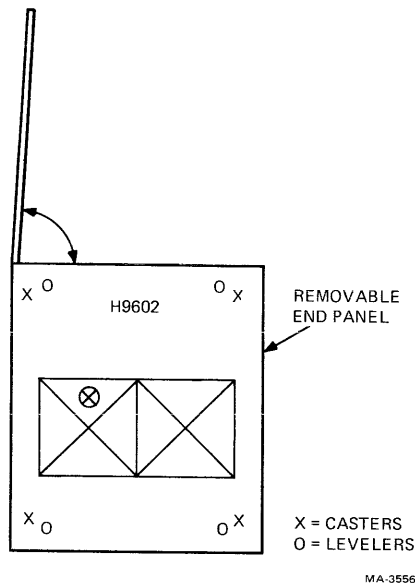


Figure 2-5 H9602 Cabinet Installation

3. Slide the sides, back, and top panels off, as one piece.

NOTE

Following step 3 will ensure that the cabinet face is not damaged. Do not ship the crating material back to the factory; it can be discarded or retained for reshipping, if reshipping is necessary.

4. Ensure that the leveling feet are above the level of the shock isolating casters (Figure 2-5).
5. Roll the cabinet(s) to the proper location for installation.

2.2.4 H9646 Cabinet Unpacking

1. Cut the binding straps and remove the bottom foam protector and top cardboard protector.

NOTE

This unit is shipped on shock isolating casters. No skid is used.

2. Roll the unit to the proper location for installation.

2.3 INSPECTION

After removing the equipment from its container, inspect it and report any damage to the responsible shipper and the local DIGITAL sales office. Inspect the equipment in the following manner.

1. Inspect all switches, indicator/switches, and panels for any obvious damage.
2. Open or remove equipment covers, where necessary, and inspect for loose or broken modules, blower or fan damage, and loose nuts, bolts, screws, and cable connections.
3. Inspect the wiring side of the logic enclosure panel (mother board assembly) for bent pins, broken wires, and any foreign material.

4. Check the transport for any foreign material that may be lodged in the take-up reel or in other moving parts.
5. Check the transport power supply to make sure the fuses and power connectors are seated properly.

2.4 TRANSPORT INSTALLATION AND CABLING

Procedures for installing and cabling the TS11 Subsystem are provided in this section.

CAUTION

For all installations, the transport must be adjacent to or bolted to the cabinets in which the M7982 is installed. A ground cable must connect the TS11 frame to the cabinet. This provides shielding for the data cable and reduces local amounts of EMI/RFI from entering the system.

2.4.1 Rackmount Installation

The TS11 AA/AB option can be installed in any standard 19 inch RETMA cabinet. Complete documentation and installation instructions are shipped with the option.

CAUTION

The TS11 AA/AB option weighs 68 kg (150 lbs). A minimum of two people are needed to move the transport to its mounting place.

NOTE

Some side skins and top covers for this style of cabinet may interfere with service clearances.

2.4.2 H960 Cabinet Installation

Proceed as follows to install a TS11 system shipped in an H960 cabinet.

1. Lower the leveling feet so that the cabinet is resting on them, not on the roll around casters.
2. Use a spirit level to level the cabinet. Make sure that all leveling feet are resting firmly on the floor.
3. Remove the shipping screws that secure the equipment to the cabinet.
4. When this cabinet is bolted to another H960 cabinet, install filler strips (Filler Strip Set, PN H952-GA) between the cabinets as shown in Figure 2-6. Make sure that the notched strip is mounted at the cabinet fronts. Tighten the bolts that secure the cabinets together and then recheck to ensure that the cabinets are level.
5. Remove the plastic shipping pin from the top of the cabinet rear access door.
6. Install a cabinet ground strap from the transport frame directly to the M7982 mounting box.
7. Replace the end panels and doors as needed.
8. Install the safety stabilizer legs to the front of the cabinet.
9. If necessary, clean all the outer surfaces.

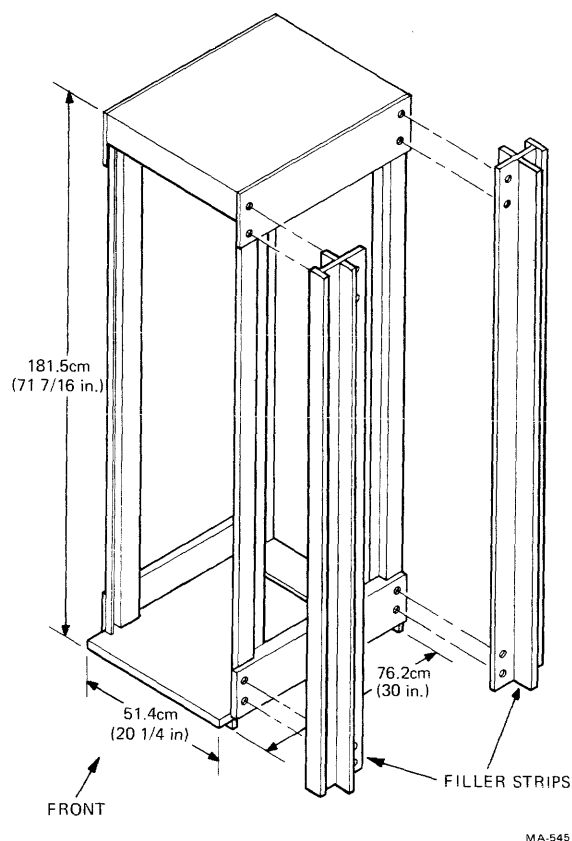


Figure 2-6 H960 Cabinet Filler Strips

2.4.3 H9602 Cabinet Installation

This section lists installation procedures for a TS11 Subsystem shipped in an H9602 cabinet.

2.4.3.1 Cabinet Disassembly – All H9602 cabinets must be disassembled before installation.

NOTE

Separate ground straps (10 gauge stranded wire) connect the front panel, end panel, and the back door to the cabinet frame. To completely remove each panel, separate the panel from the frame (instructions below), disconnect the ground strap, and completely remove the panel.

After the shipping crate has been removed, perform the following steps to disassemble the cabinet.

1. An array of vertical slots constitute venting in the cabinet front cover. A quick release latch is located approximately 2.5 cm (1 inch) behind each end of this array. Insert a thin bladed tool, such as a small steel rule, into one of the end slots. Push on the latch while simultaneously exerting a forward pull to release one corner of the front cover. In the same manner, while continuing to exert a forward pull, release the remaining latch at the other end of the array. This will totally free the front panel.
2. Leveler pads are wrapped in blister wrap and taped to the inside of the front cover. Remove the leveler pads.

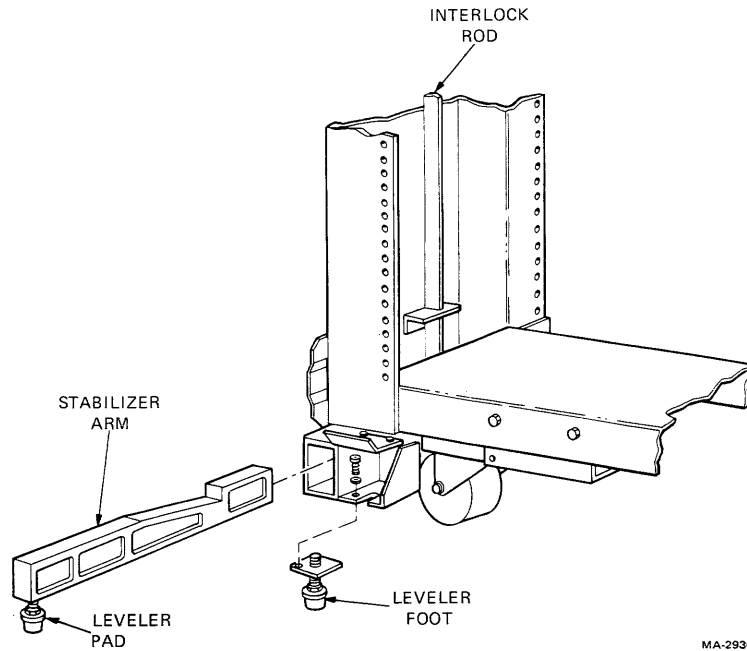


Figure 2-7 H9602 Stabilizer Leg and Leveler Feet Locations

3. Raise the interlock rods and remove the stabilizers from the stabilizer sleeve assemblies (Figure 2-7).
4. Screw the leveler pads into the stabilizers.
5. Raise the interlock rods and reinsert the stabilizers into the stabilizer sleeve assemblies (Figure 2-7).
6. Unlock the rear door using the opening tool provided for that purpose. Insert the tool in the lock and turn one quarter turn counterclockwise. Remove the door by swinging it open 90 degrees and lifting it off at the hinges.
7. Locate the fastener attached to the underside of the top cover. If any hard mounted equipment is blocking access to the underside of the top cover, the fastener was not installed. Therefore, you must proceed to step 8. If slide-mounted equipment is blocking access to the top cover, pull the stabilizer legs out until they are fully extended to the locking position. Then slide the equipment out and proceed to step 8.
8. Release the top cover by turning the fastener one quarter turn counterclockwise. When it is released, the fastener hangs by a wire from the cover support. Push the top cover forward approximately 1.27 cm (0.5 inch). Then proceed to the front of the cabinet and lift off the cover.
9. Remove one end panel by grasping it by both sides and lifting. Remove the other end panel the same way.
10. Use a Phillips screwdriver to remove the trip strips from the top, front, and rear cabinet edges.

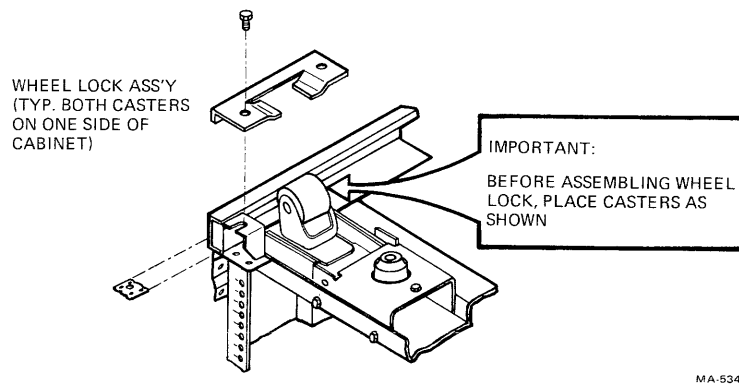


Figure 2-8 Caster Lock Assembly

2.4.3.2 Caster Locks — Caster locks (PN 7417593) are supplied with each cabinet frame (Figure 2-8). They facilitate cabinet movement by preventing two of the four cabinet casters from swiveling. They also help provide cabinet stability by restricting the direction of cabinet movement. The caster locks are mounted with hardware; they may be removed if moving the cabinet during installation becomes absolutely necessary. In any case, the locks are to be removed when the cabinet has been installed at its final destination. The locks are to be stored with the cabinet; they can be used in the future if the cabinet has to be moved.

2.4.3.3 Cabinet Leveling — Cabinet leveling is the next procedure to perform. Individual cabinets must be leveled before bolting any cabinets together. This action is necessary because of the weight differentials and self-contained shock mounts. Push the cabinets together until they adjoin. Level them as follows. (Also use this procedure for leveling a single standalone cabinet.)

1. Install the leveler feet in four places on each cabinet frame (Figure 2-7).
2. Using a 9/16 inch wrench, lower the leveler feet until all four feet on each cabinet contact the floor.
3. Adjust the highest cabinet until most of its weight is shifted from the casters to the leveler feet.
4. Using a spirit level, adjust the leveler feet until the cabinet is level.
5. Adjust the adjoining cabinet(s) to the level of the highest cabinet.

2.4.3.4 Bolting Cabinets Together — Each H9602 cabinet has four bolting plates; there are two on each side, located at the upper and lower edges. Use the following procedure to bolt cabinets together.

1. Align the bolting (middle) hole at each end of each bolting plate with the bolting hole on the plate of the adjoining cabinet.
2. After aligning the bolting holes of both cabinets, insert 1/4-20 bolts into the holes and secure them with kep nuts. (The bolts and nuts are provided.) Bolting the cabinets in this manner provides horizontal alignment.
3. After the cabinets have been bolted together, extend the stabilizer legs and lower the adjustable leveler pad on each leg until each pad touches, yet easily slides along the floor.

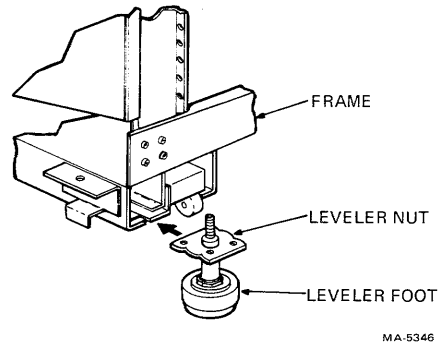


Figure 2-9 H9646 Leveler Foot Locations

2.4.3.5 Cabinet Reassembly — Reassemble each cabinet by performing the following steps.

1. Insert screws to hold the top trim strips in place.
2. Add the front and rear vertical trim strips.
3. Remount all the panels and doors in the following sequence:

End panels
 Top cover
 Rear door
 Front panel.

2.4.4 H9646 Cabinet Installation

2.4.4.1 Rear Door Removal

1. Unlock the rear door using a 5/32 inch hex key.
2. Disconnect the ground wire.
3. Unlatch the door (top latch pulled down) and lift off.

2.4.4.2 End Panel Removal

1. Remove the hinge/end panel locking brackets by loosening screws. Lift brackets off.
2. Lift panels up and away from the cabinet.
3. Remove the ground strap and save for later use.

2.4.4.3 Leveling Feet Installation

1. Assemble the leveling feet and slide them into the slot at the base of the cabinet. The slots are located on the sides (Figure 2-9).

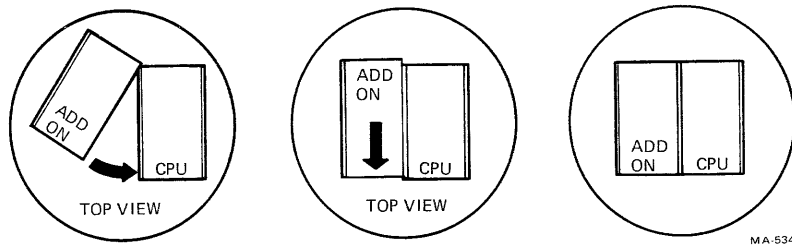


Figure 2-10 H9646 Add-on Positioning

2.4.4.4 Cabinet Leveling

1. Use a spirit level and adjust the leveler feet as required.

2.4.4.5 Cabinet Stabilizers

1. Assemble leveler foot into the stabilizer arm.
2. Install the arm into the channel located at the bottom rear of the cabinet.
3. Remove the retaining cable from the rear of the cabinet base and attach it to the rear of stabilizer arm. (This limits the forward travel of the arm.)

2.4.4.6 Bolting Cabinets Together

1. Remove the end panels where the cabinets will be joined.
2. Install the H9544-J add-on kit as follows. Screw the key buttons into the cabinet sides of both cabinets. Drop the add-on panel onto the key buttons of the stationary cabinet.
3. Roll the add-on cabinet into position (Figure 2-10) so the add-on cabinet can be pushed onto the key buttons of the stationary cabinet.
4. Pull the add-on cabinet forward to fit into the key button slots (Figure 2-10).
5. Install the front and rear interconnecting bars as shown in Figure 2-11.

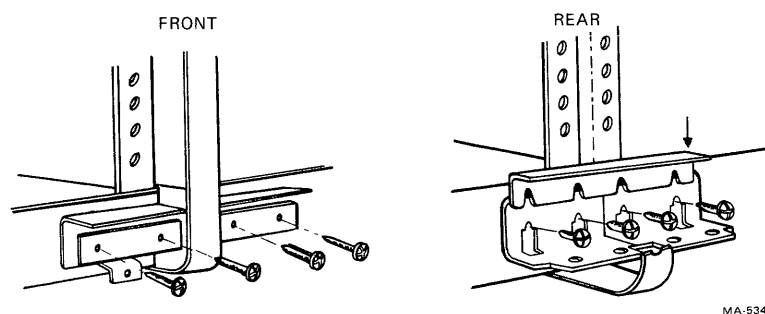


Figure 2-11 H9646 Interconnecting Bars

2.5 TS11 INTERFACE INSTALLATION

NOTE

The M8929 module must be Etch Rev. D (Circuit Schematic Rev. F) minimum to be FCC compliant.

The M7982 Unibus interface module can be placed in any small peripheral controller (SPC) slot that is wired for all Unibus signals. It accepts hex height modules and has adequate power including DD-11 series SPC backplanes in BA11 series expander boxes.

NOTE

The nonprocessor grant (NPG) jumper (CA1 to CB1) must be removed before the M7982 can perform data transfers. If the M7982 is removed from the SPC slot, insert a module that passes NPG or replace the jumper.

To install the TS11 (M7982), perform the following tasks.

1. Remove the TS11 (M7982) from its shipping container.
2. Make sure that the proper priority plug (BR5/BG5; PN 54-08778) is installed in E57 (Figure 2-12).
3. Select the proper Unibus address and interrupt vector. Use Table 2-3 as a guide.
4. Use Figure 2-12 and Table 2-4 to properly configure the address switch (E90) and interrupt vector switch (E34).

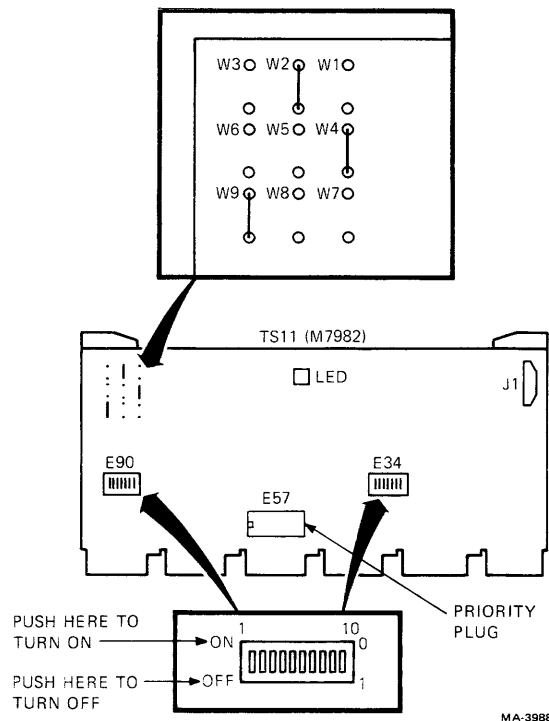


Figure 2-12 M7982 Interface Module

Table 2-3 Unibus Address and Interrupt Vectors

Number of M7982 Modules	Interrupt Vector	Unibus Address	Register
1	224	772 520 772 522	TSBA/TSDB TSSR
2	Floating (rank 37)	772 524 772 526	TSBA/TSDB TSSR
3	Floating (rank 37)	772 530 772 532	TSBA/TSDB TSSR
4	Floating (rank 37)	772 534 772 536	TSBA/TSDB TSSR

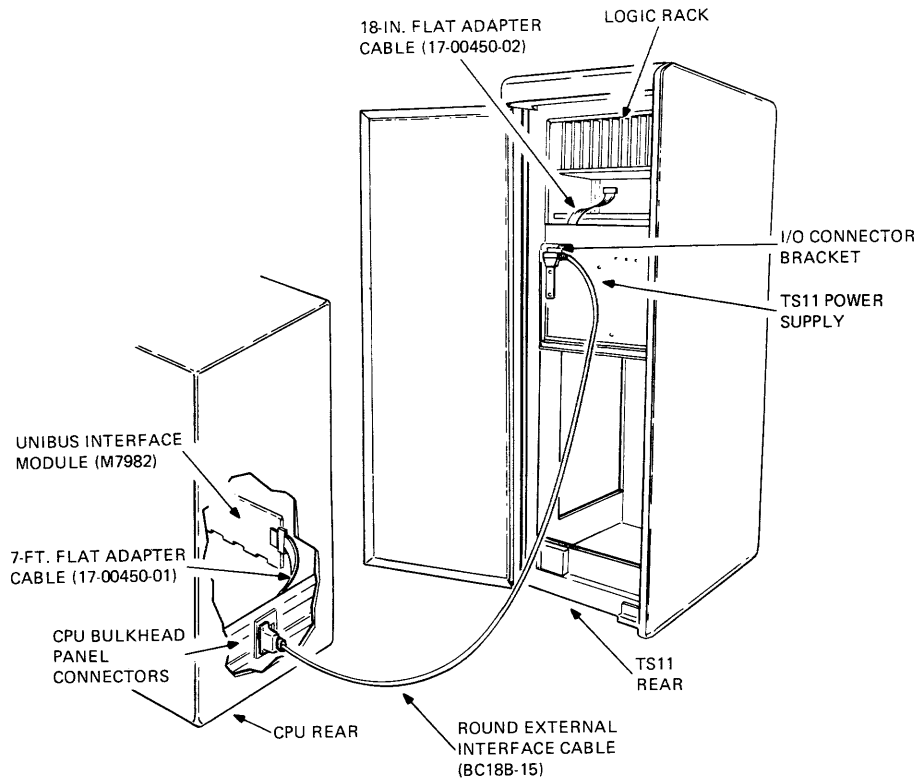
Table 2-4 Address and Vector Examples

Address																	
7			7			2			5			2			0		
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
X	X	X	X	X	1	0	1	0	1	0	1	0	1	0	0	X	X
			E34						E90								
X	X	X	X	X	1	1	10	9	8	7	6	5	4	3	2	X	X
X	X	X	X	X	off	on	off	on	off	on	off	on	off	on	on	X	X

on = 0; off = 1; X = Don't care

Vector																	
0			0			0			2			2			4		
X	X	X	X	X	X	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	2	2	2	2	2	2	2	2	2	2	2	2
X	X	X	X	X	X	X	X	X	0	1	0	0	1	0	1	X	X
												E34					
X	X	X	X	X	X	X	X	X	8	7	6	5	4	3	2	X	X
X	X	X	X	X	X	X	X	X	on	off	on	on	off	on	off	X	X

on = 0; off = 1; X = Don't care



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Figure 2-13 TS11 Signal Cabling

5. Make sure jumpers W1 through W9 are set properly as shown in Figure 2-12. W2, W4, and W9 should be set in; all others should be set out.
6. Remove the G727 bus grant card from the SPC slot.
7. Insert 7-foot CPU adapter cable (DEC PN 17-00450-01) into J1 of the interface module with red reference edge toward the handle. Figure 2-12 shows the location of J1.
8. Insert the interface module into the backplane. Use care to prevent the cable from chaffing against other modules and chassis parts.
9. Mount the 7-foot adapter cable to the CPU bulkhead (Figure 2-13).

2.5.1 Cabling

The external interface cable (BC18B-15) connects from the I/O connector bracket on rear of TS11 power supply to the CPU bulkhead. The 7-foot CPU adapter cable connects from the M7982 to the CPU bulkhead (Figure 2-13).

NOTE

The 7-foot cpu adapter cable attaches to the M7982 with the red reference edge toward the handle. The 18-inch adapter cable attaches to the motherboard with the red reference edge to the left.

Route cables to allow slack for servicing the equipment. Keep the cables away from sharp frame edges.

CAUTION

Before connecting the transport to the local power source, make sure the line voltage and frequency are compatible with transport power requirements.

Plug the power cable, supplied with the TS11 option, into a local power outlet.

Although all the internal cables are connected before shipping, Figure 2-13 provides an overview of transport cabling.

2.6 CONFIGURATION GUIDELINES

Up to four M7982 interface modules may be configured into a host system. The first M7982 has been assigned interrupt vector 224, while the second, third, and fourth are assigned vectors from the floating vector area. Therefore, it is necessary to know the next available floating vector to assign subsequent addresses.

Since the standard data cable length is 8 m (25 feet), placement of cabinets should be within 5 m (15 feet) of the host system. The standard power cable length is 2 m (6 feet) for the rackmount and 3 m (9 feet) for the cabinet options.

2.7 ACCEPTANCE TESTING

This section lists and describes all the tests and test procedures necessary to test and accept the TS11 Subsystem. When the tests are run correctly, the TS11 Subsystem is operating correctly. Detailed procedures can be found in the *TS11 Subsystem Technical Manual* and the *TS11 Pocket Service Guide*.

2.7.1 TS11 Off-Line Checkout

Off-line checkout is accomplished by successful completion of the off-line maintenance mode microdiagnostics. (These are run in auto sequence mode.) This test requires the use of a master output tape. Complete operating details and instructions are found in the *TS11 Subsystem Technical Manual* or *TS11 Pocket Service Guide*.

2.7.2 Corrective Maintenance Diagnostics

Run the TS11 Corrective Maintenance Diagnostic (MAINDEC-11-CZTSI) for one complete pass, including adjustments, as required by printouts and the program listing. Reference the *TS11 Technical Manual* or *TS11 Pocket Service Guide* for details.

2.7.3 Customer Confidence Check (Optional)

Run this check twice (with a master output tape loaded) to ensure that the transport is adjusted properly and that the transport is operational. Refer to Chapter 4 for operating instructions.

2.7.4 Performance Exerciser

Run the TS11 Data Reliability Test (MAINDEC-11-CZTSH) for 20 minutes. Reference the *TS11 Technical Manual* or *TS11 Pocket Service Guide* for details.

CHAPTER 3 USER INFORMATION

3.1 CUSTOMER RESPONSIBILITIES

The customer is directly responsible for the following tasks.

1. Obtaining operating supplies, including magnetic tape and cleaning supplies.
2. Maintaining the required logs and report files consistently and accurately.
3. Making the necessary documentation available in a location convenient to the system.
4. Keeping the exterior of the system and the surrounding area clean.
5. Ensuring that ac plugs are securely plugged in each time the equipment is used.
6. Performing the specific operations for equipment care described in Paragraphs 3.2 and 3.3 at the suggested periods, or more often if usage and environment warrant.

3.2 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; keeping tape clean is imperative.
2. Always store tape reels inside containers when the tape is not in use; keep empty containers tightly closed to guard against dust and dirt.
3. Never touch the portion of tape between the beginning of tape (BOT) and end of tape (EOT) markers; oil from fingers attracts dust and dirt.
4. Never use a contaminated reel of tape; this spreads dirt to the clean tape reels and could adversely affect tape transport reliability.
5. Always handle tape reels by the hub hole; squeezing the reel flanges leads to tape edge damage when winding or unwinding tapes.
6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.
7. Do not place magnetic tape near line printers or other devices that produce paper dust.
8. Do not place magnetic tape on top of the tape transport or in any other location where it may be affected by hot air.
9. Do not store magnetic tape near electric motors.

3.3 CUSTOMER PREVENTIVE MAINTENANCE

Digital Equipment Corporation tape transports are highly reliable precision instruments that provide years of trouble free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The following information will assist the customer in caring for equipment.

3.3.1 Preventive Maintenance

To ensure trouble free operation, a preventive maintenance schedule should be kept. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is essential to proper tape transport operation. The frequency of maintenance operations will vary with the environment and the degree to which the transport is used. Therefore, a rigid schedule for all machines is difficult to define. Cleaning after every eight hours of operation is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Paragraph 3.3.3 contains the cleaning instructions.

Before performing any cleaning operation, remove the supply reel and store it properly. When cleaning, be gentle but thorough.

CAUTION

Do not use acetone, lacquer thinner, rubbing alcohol, or trichlorethylene to clean the tape path.

3.3.2 Magnetic Tape Transport Cleaning Kit

A magnetic tape transport cleaning kit (TUC01) has been carefully assembled to provide cleaning materials that will not harm tape equipment or leave any residue to interfere with data reliability. The hints contained in the following few paragraphs will ensure that the very best results will be obtained from the kit.

The cleaning fluid in this kit is one of the best cleaners available. Unscrew the top and punch a small hole in the metal seal covering the pour spout.

WARNING

When using DECmagtape cleaning fluid, avoid excessive skin contact and contact with the eyes. Do not swallow it. Use the cleaning fluid only in a well-ventilated area.

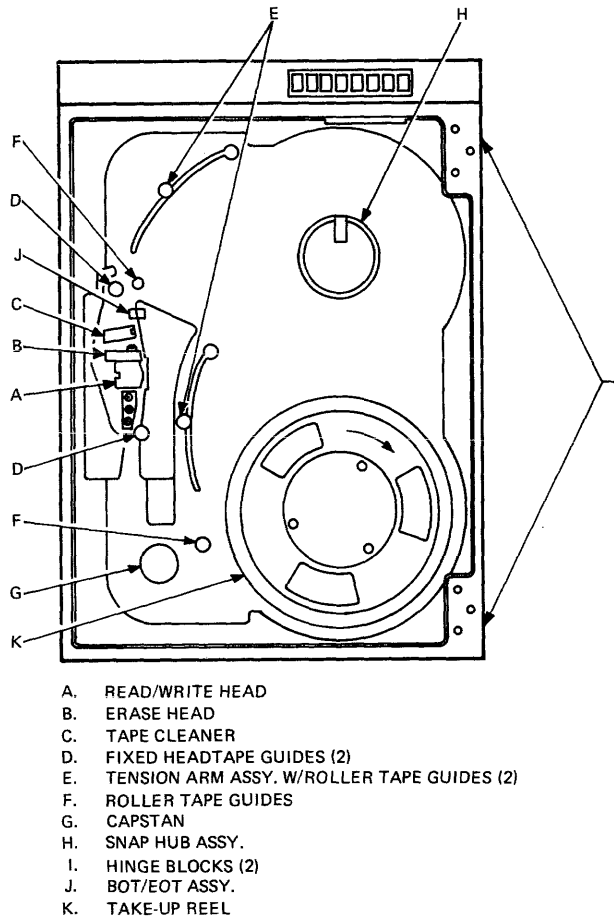
When cleaning tape equipment, never dip a dirty cleaning swab or wipe into the can. To transfer fluid onto the swab, pour a little into the screw cap and dip the swab into the cap. Discard the remaining fluid when the cleaning operation is complete.

Always keep the can of fluid tightly closed when not in use; the fluid evaporates rapidly when exposed to air.

Use the cleaning materials from the kit to clean tape heads, tape guides, tape cleaner, reel hubs, and any part of the drive, **except the capstan**, where dirty residue could ultimately contact the tape. To clean other parts of the drive, such as the exterior surfaces of doors, use any reasonably clean, lint-free material with or without cleaning fluid.

CAUTION

To clean the capstan, use only the cleaning fluid provided in the TUC01 cleaning kit. Other cleaning fluids may damage the capstan. Never use alcohol.



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Figure 3-1 Transport Components to Be Cleaned

Should you encounter any unusually stubborn dirt deposit that resists the cleaner, try a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with cleaning fluid to remove soapy residue.

3.3.3 Cleaning the TS11 Subsystem Transport

1. Dismount the tape from the unit.
2. Clean the following components of the transport using a foam-tipped swab soaked in cleaning fluid (Figure 3-1).

Read/write head (A)
 Erase head (B)
 Tape cleaner (C)
 Two fixed headtape guides (D)
 Tension arm assemblies with roller tape guide (E)
 Roller tape guide (F)

NOTE

When cleaning the roller guides, the cleaning fluid should contact only the tape-bearing surfaces. This will prevent degreasing the roller guide bearings.

3. Use cleaning fluid provided in the TUC01 Cleaning Kit with a foam-tipped swab to clean the capstan.
4. Use a lint-free wipe with a polishing action to remove any remaining deposits from the heads.
5. Finally, use a dry wipe to clean the reel-contacting metal surfaces of the upper hub. Dirt on these surfaces may cause tape reel slippage.

3.3.4 Ordering

Purchase orders for supplies, accessories or documentation should be forwarded to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). New Hampshire customers should dial (603)-884-6660. Terms and conditions include net 30 days and F.O.B. DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. Minimum order is \$35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

3.4 DIGITAL REPAIR SERVICE

Digital Field Service offers a range of flexible service plans.

ON SITE SERVICE offers the convenience of service at your site and insurance against unplanned repair bills. For a small monthly fee you receive personal service from our Service Specialists. Within a few hours the specialist is dispatched to your site with equipment and parts to give you fast and dependable maintenance.

BASIC SERVICE offers full coverage from 8 a.m. to 5 p.m., Monday through Friday. Options are available to extend your coverage to 12-, 16-, or 24-hour days, and to Saturdays, Sundays, and holidays.

DECservice offers a premium on-site service that guarantees extra-fast response and nonstop remedial maintenance. We don't leave until the problem is solved, which makes this service contract ideal for those who need uninterrupted operations.

Under Basic Service and DECservice all parts, materials, and labor are covered in full.

CARRY-IN SERVICE offers fast, personalized response, and the ability to plan your maintenance costs for a smaller monthly fee than On-Site Service. When you bring your unit to one of 160 Digital Servicenters worldwide, factory-trained personnel repair your unit within two days (usually 24 hours). This service is available on selected terminals and systems. Contact your local Digital Field Service Office to see if this service is available for your unit.

Digital Servicenters are open during normal business hours, Monday through Friday.

DECmailer offers expert repair at a per use charge. This service is for users who have the technical resources to troubleshoot, identify, and isolate the module causing the problem. Mail the faulty module to our Customer Returns Center where the module is repaired and mailed back to you within five days.

PER CALL SERVICE offers a maintenance program on a noncontractual, time-and-materials-cost basis. This service is available with either On-Site or Carry-In service. It is appropriate for customers who have the expertise to perform first-line maintenance, but may occasionally need in-depth support from Field Service.

Per Call Service is also offered as a supplementary program for Basic Service customers who need maintenance beyond their contracted coverage hours. There is no materials charge in this case.

On-Site Per Call Service is provided on a best effort basis, with a normal response time of two to three days. It is available 24 hours a day, seven days a week.

Carry-In Per Call Service is available during normal business hours, with a two to three day turnaround.

For more information on these Digital service plans, prices, and special rates for volume customers, call one of the following numbers for the location of the Digital Field Service office nearest you.

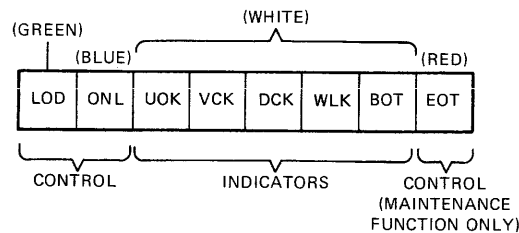
Digital International Field Service Information Numbers

U.S.A.	1-(800)-554-3333	Denmark	430-1005
Canada	(800)-267-5251	Spain	91-7334370
United Kingdom	(0256)-57122	Finland	90-423332
Belgium	(02)-242-6790	Holland	(01820)-34144
West Germany	(089)-9591-6644	Switzerland	01-8105184
Italy	(02)-617-5381/2	Sweden	08-987350
Japan	(03)-989-7161	Norway	2-256422
France	1-6873152		

CHAPTER 4 OPERATION

4.1 CONTROLS AND INDICATORS

The operator controls are located at the upper right corner of the transport (Figure 4-1). They are comprised of three lighted push buttons (colored) and five indicators (white).



LOD - LOAD
ONL - ON LINE
UOK - MICROPROCESSOR OK
VCK - VOLUME CHECK
DCK - DENSITY CHECK ERROR
WLK - WRITE LOCK
BOT - BEGINNING OF TAPE
EOT - END OF TAPE

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Figure 4-1 TS11 Transport Controls and Indicators

The controls perform a dual function: operational control and diagnostic control. The transport must be off-line for the operator to use these functions. Both features are defined in this chapter.

The operational functions of the controls and indicators are listed in Table 4-1 and 4-2, respectively.

4.2 OPERATING PROCEDURES

Transport operating procedures are described in the following paragraphs.

4.2.1 Application of Power

For rackmount variations, make sure that the transport power supply circuit breaker is in the on position. The circuit breaker is located at the rear of the frame next to the ac line cord. For cabinet mounted variations, verify the rackmount procedure above as well as the following.

1. If the power controller REMOTE ON/OFF/LOCAL ON switch is in the REMOTE ON position, transport power is controlled by the processor POWER key switch. This method is used in normal operation.

Table 4-1 Control Switch Functions

Switch	Function
LOD (Green)	<p>This control switch is the main operational switch; it has the following three functions. (Figure 4-2 diagrams these functions.)</p> <p>Loading Tape If a supply tape is correctly mounted and threaded (with tension arms not against limit switches) pressing LOD initiates the following sequence. The tape moves forward until either 7.65 m (25 ft) of tape (calculated by tachometer ticks) has been loaded or the beginning of tape (BOT) marker is sensed. If tape moves forward 7.65 m (25 ft) without sensing BOT, tape motion stops and rewinds past the BOT marker, then forward to BOT. Tape motion stops with the tape resting at BOT.</p> <p>Rewinding Tape (to BOT, prior to an unload) Pressing LOD when the tape is loaded causes tape to rewind to the BOT marker and stop.</p> <p>Unloading Tape Once the tape is rewound and resting at BOT, pressing LOD causes the tape to automatically unload from the transport tape path onto the supply reel. The tape then stops.</p> <p>NOTE: The LOD switch can be operated more than once during a cycle. For example, pressing the switch while the drive is rewinding off-line will cause the drive to unload. Pressing the switch again will cause the drive to just rewind and not unload.</p> <p>The LOD switch glows when the tape is correctly loaded.</p>
ONL (Blue)	<p>This is a locking switch which puts the transport on- and off-line. Pushing it in (locking it) puts the transport on-line. Pushing it again unlocks the switch and puts the transport off-line. This switch is inoperative when the LOD switch indicator is off. The ONL switch glows when the transport is on-line.</p>
EOT (Red)	<p>This switch controls several maintenance functions. The only use in user-mode function is the customer confidence check, described later in this chapter. Pushing this button, when in non-maintenance mode and/or when a microdiagnostic error is displayed causes the microprocessor to restart.</p>

Table 4-2 Operation Indicators

Indicator	Definition
UOK (White)	Microprocessor OK: This indicator glows when the control microprocessor is operating with no errors.
VCK (White)	Volume Check: VCK lights when any change in status occurs (going off-line or on-line; reinitializing the microprocessor).
DCK (White)	Density Check: This indicator glows if a valid identification burst (IDB) is not seen at BOT. (The tape can still be read if it is the correct density.) If writing, DCK causes a tape position lost class error because the IDB was not written properly.
WLK (White)	Write Lock: This indicator glows if no tape reel is mounted, or if a reel is mounted without a write-enable ring.
BOT (White)	Beginning of Tape: This indicator glows when the BOT marker is positioned over its sensor.
EOT (Red)	End of Tape: This indicator glows when the tape has been moved past the EOT marker. The subsystem software initialize command resets the EOT bit regardless of the tape position.
<p>NOTE: Manually moving tape past the EOT marker will not cause the indicator to come on.</p>	

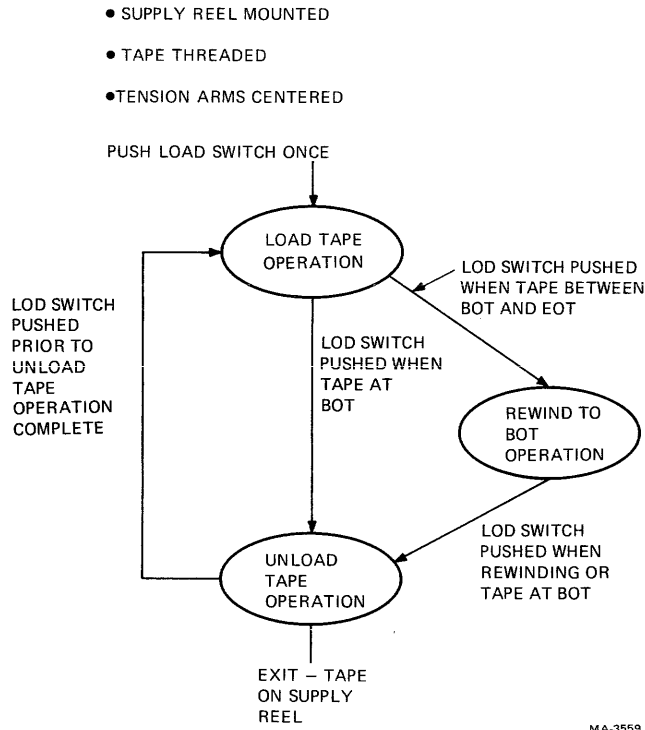


Figure 4-2 Load Switch State Diagram

2. If the processor POWER key switch is not activated, transport power may be turned on locally by setting the power controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON. This method may be used during maintenance.

4.2.2 Loading and Threading Tape

Use the following procedure to mount and thread magnetic tape.

1. Apply power to the transport. Make sure that the transport is off-line (the ONL indicator does not glow).
2. Place a write enable ring in the tape reel groove if data is to be written on the tape. Make sure that no ring is in the groove if data on the tape is not to be erased or written over.
3. Mount the supply reel onto the upper hub in the following manner. Release the snap lock lever on the upper hub by pulling it firmly outward on the rim end. Then, with the reel groove facing away from the operator, mount the supply reel onto the upper hub.

When the reel is firmly seated and flat against the hub flange (press the reel firmly and evenly, but not heavily), close the snap lock lever on the hub. The supply reel is now correctly mounted. If the reel wobbles when turning, it is not seated flat against the hub flange.

4. Manually unwind tape from the file reel and thread the tape by the tape guides and head assembly. (Refer to Figure 4-2.)

- Wind approximately four turns of tape onto the take-up reel. Make sure that the tape is seated in the tape guides.

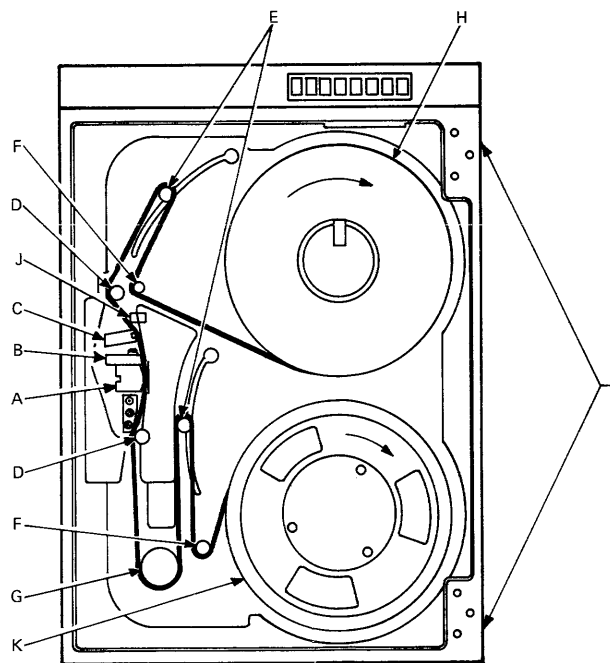
CAUTION

Wind the tape flat onto the take-up reel. Do not bend the tape back or place the tape end outside of the reel. When winding tape onto the take-up reel, simultaneously unwind the supply reel to relieve tension on the tape. Rotate the reels gently. Do not jerk the tape, since this could cause the tape to stretch.

- Before loading tape, the tension arm roller guides must be located between stops (Figure 4-3). Close the front door assembly to allow the tape load sequence to occur. Press the LOD switch and the seek for BOT sequence will begin. This sequence consists of moving tape forward to the BOT marker. If a BOT marker is not found within 7.65 m (25 feet), the tape will rewind to the BOT marker. If a BOT marker was not present or sensed, the tape will unload. When the BOT marker is sensed, tape motion stops and the BOT indicator glows. The tape is now positioned at the load point (BOT marker) and the transport is ready for use.

NOTE

The front door assembly must be closed to allow the tape to load.



- A. READ/WRITE HEAD
- B. ERASE HEAD
- C. TAPE CLEANER
- D. FIXED HEADTAPE GUIDES (2)
- E. TENSION ARM ASSY. W/ROLLER TAPE GUIDES (2)
- F. ROLLER TAPE GUIDES
- G. CAPSTAN
- H. SUPPLY REEL AND SNAP HUB ASSY.
- I. HINGE BLOCKS (2)
- J. BOT/EOT ASSY.
- K. TAKE-UP REEL

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Figure 4-3 Tape Loading Path

7. Press the ONL switch to put the transport on-line. If you pressed the switch while the load sequence was in motion, the on-line indicator will glow when the tape motion stops.

4.2.3 Unloading Tape

Depending on whether or not the tape is at the BOT marker, use one of the following unloading procedures.

4.2.3.1 Tape Loaded, Not at BOT

1. Make sure the transport is off-line.
2. Press the LOD switch. The transport should execute a high speed rewind operation. When the BOT marker is sensed, tape motion stops. (Goes past, then forward, and stops at BOT.)
3. Press the LOD switch again. (It may be pressed during rewind operation.) An unload sequence begins with the tape gently winding onto the upper supply reel. When the tape runs off the take-up reel, motion stops.
4. Manually wind the remaining tape onto the supply reel. If you wish to remove the supply reel, unlock the snap lock lever on the hub and gently pull the reel off.

4.2.3.2 Tape Loaded, at BOT

1. Make sure the transport is off-line.
2. Press the LOD switch. The unload sequence begins with the tape gently winding onto the upper supply reel. When the tape runs off the take-up reel, motion stops.
3. Manually wind the remaining tape onto the supply reel. If you wish to remove the supply reel, unlock the snap lock lever on the hub and gently pull the reel off.

4.2.4 Restart After Power Failure

In the event of a power failure, the transport automatically shuts down and tape motion stops without any physical damage to the tape. If the on-line switch was on, the transport performs an auto-load sequence. If the on-line switch was off, the transport stays unloaded and off-line.

4.2.5 Restart After Fail-Safe

If, for some reason, either tension arm limit is exceeded, causing a fail-safe condition, tape motion automatically stops without damaging the tape. When this fail-safe condition occurs, the transport does not respond to either on-line or off-line commands. To restart the transport follow the load tape procedure.

NOTE

Before restarting, this failure should be recorded in the system log with an indication of which fail-safe switch was exceeded. This information will aid Field Service in resolving the problem should the fail-safe condition be due to a tape transport problem.

4.3 OPERATOR TROUBLESHOOTING

Before any maintenance personnel are called to correct a problem, the operator can make a few minor checks and possibly avoid a service call. The following precautions may isolate an easily correctable error.

1. If the tape does not stop at BOT, make sure the tape has a BOT marker.

2. If a write operation is to be performed, make sure that the write enable ring is inserted in the tape reel.
3. If problems are related to the transport's read/write, clean the tape path according to the daily (eight hour) preventive maintenance procedures listed in Chapter 3.
4. Verify that the circuit breaker on the back of the TS11 power supply is on.
5. If the transport does not power up for cabinet mounted variations, make sure the power controller circuit breaker is on. Also make sure that the REMOTE ON/OFF/LOCAL ON power controller switch is in the REMOTE ON position.
6. Make sure the front door is closed.

4.4 CUSTOMER CONFIDENCE CHECK

The customer confidence check verifies the transport's operating characteristics. The test consists of several transport resident diagnostics that run sequentially and automatically once initiated.

4.4.1 Running the Customer Confidence Check

CAUTION

This test reads and writes on tape; therefore, it is necessary to remove any currently mounted tape to save the data on it.

An industry standard master output tape (also known as standard amplitude tape) that is known to be good must be used to prevent media related defects from registering as hardware problems. This tape is provided as part of a Digital Maintenance Agreement. Nonservice contract customers may obtain the tape through the Digital Accessories and Supplies Group by ordering PN 29-11696. Ordering information is given in Section 3.3.4.

Run the customer confidence check by performing the following steps.

1. Make sure the master output tape has a write enable ring inserted in the back of the supply reel.
2. Mount and load the tape. Make sure the load light is on.
3. Make sure that the WLK light is off; leave the drive off-line.
4. Push the leftmost (LOD) and rightmost (EOT) operator panel pushbuttons at the same time.

The operator panel will indicate that the test is ready to run by lighting the two leftmost indicators (LOD, ONL).

5. Pressing the ONL switch once will start the test. Let the test run to completion, then press the switch again to stop the test and return the machine to normal operation. If the test is passed, the indicators display a rotating pattern of left-shifting 1s and 0s. If a test is failed, its specific test number will blink in the operator panel indicators. These panel indicators represent a binary register whose octal value is the failing test number. Clean the tape transport as described in Chapter 3 and try the test again. If the test is still failed, record the new failing test number and contact your local service representative.

CHAPTER 5 PROGRAMMING

5.1 TS11 REGISTERS

This chapter describes and defines the TS11 registers and packet processing. In addition, programming examples and packet formats are provided to illustrate basic TS11 programming concepts.

It is important to understand that command and data packets are used to transfer command and data information to the transport. The traditional method of writing a command or data word to a Unibus register is not used. A command packet consists of a command word and up to three additional words of command modifiers or qualifiers. This command packet is assembled in host CPU memory space on modulo-4 memory addresses. The beginning address of the command packet is the command pointer. Only the high 16-bits of an 18-bit word are used. This pointer is used by the controller to NPR transfer the command packet to the subsystem.

The eight TS11 (M7982) registers are:

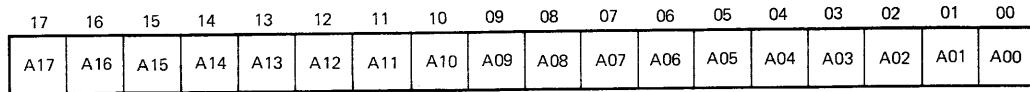
TSBA	(1)	– Unibus Address Register
TSDB	(1)	– Unibus Data Buffer
TSSR	(1)	– Status Register
XST	(5)	– Extended Status Registers

5.1.1 TSBA (Unibus Address Register – Base Address – Read Only)

The TSBA is an 18-bit register. It is parallel loaded from the TSDB every time the TSDB is loaded as a Unibus slave by the CPU. TSDB bits 15-2 load into TSBA bits 15-2; and TSDB bits 1 and 0 load into TSBA bits 17 and 16. Zeros are loaded into TSBA bits 1 and 0. TSBA bits 17 and 16 are displayed in TSSR bits 9 and 8 respectively. TSBA can be instructed by the transport to increment or decrement by two for nonprocessor request (NPR) word transfers, or by one for NPR byte transfers. The TSBA is the base address in the read only mode and it is not cleared on power up, subsystem INIT, or bus INIT. It can also be read at any time with or without the drive unit connected.

The TSBA register is illustrated in Figure 5-1 and the bits are listed and defined in Table 5-1. The TSBA register serves the following two major purposes.

1. The TSBA can be used as a command and message pointer to the remote transport device registers (command and message buffers). These are located somewhere in the Unibus address space. The content, loaded into TSDB when the M7982 is the bus slave, is considered the command or message pointer. In this mode, the M7982 receives data (initiated by the transport) at this command pointer address and sends it to the transport for storage and/or execution. The message buffer address tells the M7982 where to place the message sent to the CPU address space. When used as a message pointer, the highest message buffer address + 2 is left in the TSBA.
2. The TSBA can be used as a data pointer (NPR's bus address 0), pointing to data buffer areas located somewhere in the Unibus address space. [In this mode, the transport will serially load the TSDB with data (18 address bits); TSDB bits 17 through 0 load into TSBA



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Figure 5-1 TSBA Register

Table 5-1 TSBA Bit Definitions

Bit	Name	Definition
17	A17	Bus address bit 17
16	A16	Bus address bit 16
15	A15	Bus address bit 15
14	A14	Bus address bit 14
13	A13	Bus address bit 13
12	A12	Bus address bit 12
11	A11	Bus address bit 11
10	A10	Bus address bit 10
09	A09	Bus address bit 09
08	A08	Bus address bit 08
07	A07	Bus address bit 07
06	A06	Bus address bit 06
05	A05	Bus address bit 05
04	A04	Bus address bit 04
03	A03	Bus address bit 03
02	A02	Bus address bit 02
01	A01	Bus address bit 01
00	A00	Bus address bit 00

bits 17 through 0, but bits 17 and 16 are displayed in TSSR bits 9 and 8, respectively.] The contents of TSBA are then used to point to data buffer areas while the M7982 transfers data by NPRs.

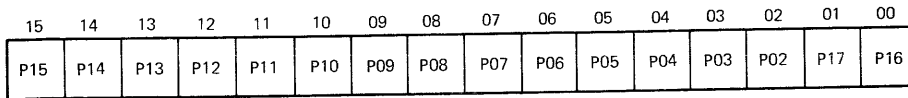
5.1.2 TSDB (Unibus Data Buffer Register – Base Address – Write Only)

The TSDB is an 18-bit register that is parallel loaded from the Unibus or serially loaded from the transport. A 16-bit portion of this register is used as a word buffer register to the M7982 when the M7982 is the bus slave (for beginning an operation). The same word buffer register is also used by the transport (for data during NPR transfers) when the M7982 is bus master. The TSDB can be loaded when the M7982 is bus slave by three different transfers from a bus master. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte). The third transfer is for normal (word) operation (DATO). This register is write only and is not cleared at power up, subsystem initialize, or bus initialize. It cannot be loaded without the complete transport unit connected and a serial bus synchronous clock. The M7982 responds with Ssyn any time the TSDB is written to.

The TSDB register is illustrated in Figure 5-2 and the bits are listed and defined in Table 5-2.

5.1.2.1 Normal Operation – When TSDB is loaded by a DATO (write a word to TSDB) the following happens. Bit 0 and bit 1 are loaded with zeroes. Bits 2 through 15 are loaded with bits 2 through 15, respectively, from the Unibus. Bits 16 and 17 are loaded from bits 0 and 1, respectively, from the Unibus. The bus address is 16XXXX, where XXXX can be any unused address from 0 through 1776. The M7982 indicates to the transport a TSDB word load when the M7982 is bus slave.

5.1.2.2 Data Wraparound Internal to the M7982 (Diagnostic Mode) – When TSDB is loaded by a DATOB to TSDB high byte, the following happens. Bits 0 through 7 are loaded with bits 8 through 15, respectively, from the Unibus. Bits 8 through 15 are loaded with bits 8 through 15, respectively,



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Figure 5-2 TSDB Register
(Loaded With a Command Pointer)

Table 5-2 TSDB Bit Definitions

Bit	Name	Definition
15	P15	Command pointer bit 15
14	P14	Command pointer bit 14
13	P13	Command pointer bit 13
12	P12	Command pointer bit 12
11	P11	Command pointer bit 11
10	P10	Command pointer bit 10
09	P09	Command pointer bit 09
08	P08	Command pointer bit 08
07	P07	Command pointer bit 07
06	P06	Command pointer bit 06
05	P05	Command pointer bit 05
04	P04	Command pointer bit 04
03	P03	Command pointer bit 03
02	P02	Command pointer bit 02
01	P17	Command pointer bit 17
00	P16	Command pointer bit 16

from the Unibus. Bits 16 and 17 are loaded with bits 8 and 9 respectively, from the Unibus. The TSDB is then loaded into TSBA. The bus address is 16XXXX (odd). This transfer will be executed anytime a DATOB to the TSDB high byte is done. If SSR (see TSSR bit 07) is clear, an error (RMR TSSR bit 12) occurs, but the transfer is still executed and completed. The TSSR is not affected (except for SSR bit 07, which gets cleared). The TS11 tells the transport over the serial bus to stop the transport from updating TSSR. To use the transport again, the M7982 must initialize the transport (that is, write the TSSR).

5.1.2.3 Data Wraparound External With Transport — When TSDB is loaded by a DATOB to TSDB low byte, the following happens. Bits 0 through 15 are loaded with bits 0 through 15, respectively, from the Unibus. (Most PDP-11 CPUs assert all zeroes for bits 8 through 15 except for a MOV_B; this sign extends bit 07. See the respective processor handbook for a MOV_B instruction.) Bits 16 and 17 cannot be determined. The bus address is 16XXXX (even). The M7982 sends TSDB bits 0 through 15 and a qualifier to the transport.

The transport returns the same data and another qualifier which instructs the M7982 to load the TSDB bits 0 through 17 into TSBA bits 0 through 17, respectively, and to load bits 0 through 15 into TSSR bits 0 through 15, respectively. (Some bits cannot be loaded; see the TSSR register description which follows.) The M7982 then returns a serial bus transfer complete to the transport. To use the transport again, the M7982 must initialize the transport (that is, write the TSSR).

5.1.3 TSSR (Status Register – Base Address + 2 – Read/Write)

The TSSR is a 16-bit register that can only be updated from the transport or internal M7982 logic; it cannot be modified from the Unibus except for SPE, UPE, RMR, NXM, and SSR bits that are cleared when the TSDB is written by the host CPU. It is a read/write register at base address

16XXXX+2. (The DATO/DATOB write transfers cause the M7982 to modify 16XXXX+2.) It can be read at any time with or without the transport unit connected. The bit positions are illustrated in Figure 5-3 and described in Table 5-3.

Table 5-3 TSSR Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	SC	S	Special Condition: When set, this bit indicates that the last command was not completed without incident. Specifically, either an error was detected or an exception condition occurred. An exception condition could be a tape mark on read commands, reverse motion at BOT, EOT while writing, etc.
14	UPE	4/5	Unibus Parity Error: This bit is set by the M7982 when it detects a parity error in the memory data being transferred from the CPU memory.
13	SPE	7F2	Serial Bus Parity Error: This bit is set by the M7982 when it detects a serial bus parity error on data received from the transport. 7F2 means termination class 7 and fatal class 2.
12	RMR	S	Register Modification Refused: This bit is set by the M7982 when a command pointer is loaded into TSDB and subsystem ready (SSR) is not set. This bit may set on a bug free system if ATTN interrupts are enabled.
11	NXM	4/5	Nonexistent Memory: This bit is set by the M7982 when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet.
10	NBA	S	Need Buffer Address: When set, this indicates that the transport needs a message buffer address. This bit is cleared during the set characteristics command if the transport gets valid data; it is always set after subsystem initialization.
09	A17	S	Bus Address Bit 17: A17 and A16 (bits 08 and 09) display the values of bits 17 and 16 in the TSBA register.
08	A16	S	Bus Address Bit 16: See A17 above (bit 09).
07	SSR	S	Subsystem Ready: When set, this bit indicates that the TS11 Subsystem is not busy and is ready to accept a new command pointer.
06	OFL	S	Off-Line: When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.
05	FC1	7	Fatal Termination Class 01: FC1 and FC0 (bits 05 and 04) are used to indicate the type of fatal error that has occurred on the transport. These bits are valid only when SC is set and the termination class code bits are all set (111). Refer to special conditions and errors, Section 5.3.3 of this manual.
04	FC0	7	Fatal Termination Class 00: See FC1 (bit 05) above.
03	TC2	S	Termination Class Bit 02: This bit, along with the TC1 and TC0 bits, acts as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The conditions in each class have similar significance and, as applicable, recovery procedures. The code provided in this field is expected to be utilized as an offset into a dispatch table for handling the condition. These bits are valid only when special condition (SC) is set. Refer to special conditions and errors Section 5.3.3 of this manual.
02	TC1	S	Termination Class Bit 01: See TC2 (bit 03) above.
01	TC0	S	Termination Class Bit 00: See TC2 (bit 03) above.
00	-	-	Not used.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC S	UPE 4/5	SPE 7F2	RMR S	NXM 4/5	NBA S	A17 S	A16 S	SSR S	OFL S	FC1 7	FC0 7	TC2 S	TC1 S	TC0 S	

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Figure 5-3 TSSR Register

TSSR register bits 14 through 11 and 7 are cleared only on system power up, TS11 power up, subsystem initialize, or at the beginning of any write command to the TSSR register. Bits 15 and 7 are also under control of the transport. These may be set or cleared independently of any TS11 operation. Bits 10 and 6-0 are exclusively controlled by the transport and reflect the transport status as indicated.

NOTE

Any write function to the M7982 base address 16XXXX+2 is decoded as a subsystem initialize. This resets the TS11 and transport no matter what state they are in and causes an automatic load sequence returning the tape to BOT if the transport is on-line.

The TSSR register utilizes several bits to increase its status reporting capabilities. TSSR bits 4 and 5 report four fatal class error codes and TSSR bits 1, 2, and 3 report seven termination class status codes. Fatal error bits are valid only if the termination class equals 7.

On fatal errors (fatal class bits equal seven), if the need buffer address is not set (NBA=0), then the message may be valid. If the need buffer address is set (NBA=1,) then there was no message.

The RMR bit will not affect the error class codes because RMR may occur on a bug free system. However, RMR will set the special condition (SC). (You may have tried to perform the next command while the drive was outputting the ATTN MSG.) If RMR is seen in the TSSR, the CPU must have written the TSDB while the command was executing.

NOTE

The TSSR may not reflect the current state of the hardware if ATTNs are not enabled and the message buffer is not released. (That is, the drive may be off-line while the TSSR shows on-line). To keep the TSSR up to date would violate message packet protocol.

Fatal Class Codes

TSSR

Bits

5 and 4

Description

0-0

Internal microdiagnostic failure in diagnostic mode or capstan runaway in operational mode (337 octal in operator panel)

See the fatal error code byte (XSTAT3) for the diagnostic function

Cleared by drive initialize command or subsystem initialize

Subsequent tape operations will not be accepted (command reject) until, as a minimum, a drive initialize is issued

0-1	I/O sequencer CROM parity error Cleared by drive initialize or subsystem initialize
1-0	Microprocessor CROM parity error, I/O silo parity error, serial bus parity error, or other fatal error Cleared only by subsystem initialize
1-1	Low ac or loss of ac power has been detected and a power down is in effect Cleared only by subsystem initialize

NOTE

TSSR is not cleared immediately after initialization. The microprocessor runs to complete an automatic load sequence. When tape is at BOT, TSSR updates.

Termination Class Codes

**TSSR
Bits
3,2,1**

	Description
000	Normal termination
001	Attention condition
010	Tape status alert
011	Function reject
100	Recoverable error (tape position = one record down from start of function)
101	Recoverable error (tape not moved)
110	Unrecoverable error (tape position lost)
111	Fatal controller error (see Fatal Class bits)

5.1.4 XST (Extended Status Registers)

Five additional registers are employed to provide additional status information: residual frame count register (RBPCR) and extended status register 0, 1, 2, and 3. These registers are illustrated in Figure 5-4 and the bits are defined in Tables 5-4 through 5-8.

The extended status registers are not read directly from the registers accessible at the Unibus interface. At the end of a command or by issuing a Get Status Command the message packet information is updated. The end message packet which results from the get status contains the extended status words. This means that a message buffer has to be defined to the subsystem before the extended status registers are available to the software.

5.1.5 TS11 Register Summary

Figure 5-4 is a summary of the TS11 registers.

REGISTER	BITS															
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TSBA (R/O)	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
TSDB (W/O)	P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P16
TSSR	SC	UPE	SPE	RMR	NXM	NBA	A17	A16	SSP	OFL	FC1	FC0	TC2	TC1	TC0	
	S	4/5	7/F/2	S	4/5	S	S	S	S	S	7	7	S	S	S	
RBPCR	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00
XST0	TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
	S/2	2	2	2	3/6	3	3	3	S	S/1/3	S	S/3	S	S/3/6	S/2/3	S/2
XST1	DLT		COR	CRS	TIG	DBF	SCK		IPR	SYN	IPO	IED	POS	POL	UNC	MTE
	4		S	4	4	4	4		S/4	4	S/4	4	S/4	4	4	4
XST2	OPM	SIP	BPE	CAF		WCF		DTP	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	S	7F2	7F2	7		7		S	S	S	S	S	S	S	S	S
XST3	MICRODIAGNOSTIC ERROR CODE								LMX	OPI	REV	CRF	DCK	NOI	LXS	RIB
	7	7	7	7	7	7	7	7	6	6	S	7	S/6	6	6	2

Termination Class Codes:

- 0 = Normal Termination
- 1 = Attention Condition
- 2 = Tape Status Alert
- 3 = Function Reject
- 4 = Recoverable Error - Tape Position = One record down tape from start of function
- 5 = Recoverable Error - Tape not removed
- 6 = Unrecoverable Error - Tape position lost
- 7 = Fatal Controller Error

Fatal Class (FC) Codes (in TSSR):

- 0 = Internal diagnostic failure (displayed in OP panel)
- 1 = IO sequencer CROM parity error or main CROM parity error (if PC = 1750 then error is I/O CROM parity).
- 2 = Microprocessor CROM parity error or other fatal error (Program counter display or SILO parity in ext. status)
- 3 = Loss of AC power has been detected.

Non-termination Class Code:

S = Status

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Figure 5-4 TS11 Register Summary

Table 5-4 RBPCR Bit Descriptions

Bit	Name	Description
15-0	C15-C0	This word contains the octal count of residual bytes, records, tape marks for the read, space records, and skip tape mark commands. The contents are meaningless for all other commands.

Table 5-5 XSTAT0 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	TMK	S/2	Tape Mark Detected: This bit is set when a tape mark is detected during a read, space, or skip command and as a result of the write tape mark or write tape mark retry commands.
14	RLS	2	Record Length Short: This bit indicates one of the following three cases. The record length was shorter than the byte count on read operations. A space record operation encountered a tape mark or BOT before the position count was exhausted. Or, the third possibility, a skip tape marks command was terminated by encountering BOT or a double tape mark (if skip tape marks command is enabled, see LET) before exhausting the position counter.

Table 5-5 XSTAT0 Bit Definitions (Cont)

Bit	Name	Causes Termination Class (TC)	Definition
13	LET	2	Logical End of Tape: This is set only on the skip tape marks command under two conditions: when either two contiguous tape marks are detected or when moving off BOT and the first record encountered is a tape mark. The setting of this bit will not occur unless this mode of termination is enabled through use of the set characteristics command.
12	RLL	2	Record Length Long: When set, this bit indicates that the record read was longer than the byte count specified.
11	WLE	3, 6	Write Lock Error: When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write enable ring. When set, TC6 indicates the WRT LOCK switch was activated during write operation.
10	NEF	3	Non-Executable Function: When set, this bit indicates that the command could not be executed due to one of the following conditions. The command specified reverse tape direction but the tape was already positioned at BOT. A motion command was issued without the clear volume check (CVC) bit being set while the volume check bit was set. A motion command was issued when the transport was off-line. A write command was issued when the tape did not contain a write enable ring [write lock status (WLS)].
09	ILC	3	Illegal Command: This bit is set when a command is issued and either its command field or its command mode field contains codes not supported by the transport.
08	ILA	3	Illegal Address
07	MOT	S	Capstan is moving.
06	ONL	S/1/3	On-Line: When set, this bit indicates that the transport is on-line and operable. It causes a TC1 on ATTN interrupt or a TC3 for a non-executable function if rejected because the transport was off-line.
05	IE	S	Interrupt Enable: This bit reflects the state of the interrupt enable bit supplied on the last command.
04	VCK	S/3	Volume Check: This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization.
03	PED	S	Phase Encoded Drive: When set, this bit indicates that the transport is capable of reading and writing only 1600 bit/in phase encoded data. It should always be set.
02	WLK	S/3/6	Write Locked: When set, this bit indicates that the mounted tape reel does not have a write enable ring installed. Therefore the tape is write protected.
01	BOT	S/2/3	Beginning of Tape: When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape. This causes TC2 if reversed in BOT, and TC3 if at BOT when a reverse command occurs.
00	EOT	S/2	End of Tape: This bit is set whenever the tape is positioned at or beyond the end of tape reflective strip. It is not reset until the tape passes over the reflective strip in the reverse direction under program control. Subsystem initialization always resets this bit (status on read, TC2 on a write). Manually moving EOT mark over the EOT sensor will not set or reset the EOT bit.

Table 5-6 XSTAT1 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	DLT	4	Data Late: This bit is set when the I/O silo is full on a read or empty on a write. The conditions occur whenever the Unibus latency exceeds the transport's data transfer rate for a significant number of transfers.
14	-	-	Not used.
13	COR	S	Correctable Data: This bit is set when a correctable data error has been encountered (on a read command only). It will not cause a termination class error but there is a dead track. Dead track bits will indicate the error. This is used primarily as a diagnostic feature.
12	CRS	4	Crease Detected: This bit is set when eight of nine data tracks go dead for less than 0.1 inches before a valid postamble is detected.
11	TIG	4	Trash In The Gap: This bit is set when non-erased data is detected in a gap during a read, write, write tape mark, or erase command.
10	DBF	4	Deskew Buffer Fail: This bit is set when one of the deskew buffers fails to set output ready within 20 microseconds after being enabled. The dead track bits indicate on which tracks this failure occurred. This error is probably a result of a broken formatter.
09	SCK	4	Speed Check: This bit is set when average tape speed varies more than five percent during a write operation.
08	-	-	Not used.
07	IPR	S,4	Invalid Preamble: This bit is set if the preamble is shorter than 36 characters or longer than 44 characters. It is also set if the preamble is incorrectly encoded beyond the fifteenth character in read or the tenth character in read after write. It is status on read, TC4 on a write.
06	SYN	4	Synchronization Failure: This bit is set if the formatter is unable to achieve synchronization in the preamble.
05	IPO	S/4	Invalid Postamble: This bit is set during read or write if any of the first 39 characters of the postamble are not read correctly. It is status on read, TC4 on a write.
04	IED	4	Invalid End of Data: This bit is set when eight out of nine tracks go dead before the postamble is detected.
03	POS	S/4	Postamble Short: This bit is set during a read or write when fewer than 38 all-zero characters are read following the all-one characters. It is status on read, TC4 on a write.
02	POL	4	Postamble Long: This bit is set during read or write operations when the postamble exceeds 42 characters.
01	UNC	4	Uncorrectable Data: This bit is set when a parity error occurs without a corresponding dead track indication. This bit is a normal write error for any dead track.
00	MTE	4	Multitrack Error: This bit is set if more than one dead track occurs in the preamble or in the data field.

Table 5-7 XSTAT2 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	OPM	S	Operation In Progress (Tape moved)
14	SIP	7F2	Silo Parity Error: This bit causes fatal class two (FC2) because the error might have occurred during the transmission of the message packet.
13	BPE	7F2	Serial Bus Parity Error At Drive: This bit is set at the transport when a parity error is detected on data transmitted from the M7982 to the transport. It causes FC2 because the error might have occurred during the transmission of the command packet.
12	CAF	7	Capstan Acceleration Fail: This bit is set if, after acceleration of tape for 45 ticks (0.5 inches), the tape speed was checked and found out of tolerance by more than ten percent (averaged over 8 ticks).
11	-	-	Not used.
10	WCF	7	Write Card Fail: This bit is set if the write card did not empty the I/O silo. This error can be the result of the write board clock not being turned on.
09	-	-	Not used.
08	DTP	S	Dead Track Parity: This bit indicates which tracks went dead, if any, during the last data transfer operation. If deskew buffer fail (DBF) is set, these bits indicate which channel failed.
07	DT7	S	Dead track 7 (See DTP)
06	DT6	S	Dead track 6 (See DTP)
05	DT5	S	Dead track 5 (See DTP)
04	DT4	S	Dead track 4 (See DTP)
03	DT3	S	Dead track 3 (See DTP)
02	DT2	S	Dead track 2 (See DTP)
01	DT1	S	Dead track 1 (See DTP)
00	DT0	S	Dead track 0 (See DTP)

NOTE: On the write characteristic command, bits 07 through 00 contain the microcode revision level; on the get status command, these bits contain the residual capstan tick count (the number of ticks from the ideal stopping point; useful for diagnostics).

Table 5-8 XSTAT3 Bit Definitions

Bit	Name	Causes Termination Class	Definition
15-08	-	7	Microdiagnostic Error Code: There is one operational error, 337 or left justified to 157400 in a 16-bit register (capstan runaway), which is displayed here. This means that the capstan was commanded to stop but exceeded the allowable stopping window. Drive must be initialized to be used for tape motion again.
07	LMX	6	Limit Exceeded: This bit is set when the tape tension arms have exceeded their allowable travel during an operation and have caused the activation of the limit switches. No tension exists on the mounted tape.
06	OPI	6	Operation Incomplete: This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after four feet of tape.
05	REV	S	Reverse: This bit is set when the direction of current tape operation is reverse. For multi-function retry commands, if at least one of the commands is reverse, the bit is set.
04	CRF	7	Capstan Response Fail: This bit is set if the capstan logic is commanded to move, but no tachometer pulses are received within five milliseconds.
03	DCK	S/6	Density Check: The current operation will be done. However, note that read, space, and skip operations will complete without error (if no other errors occur) to allow tapes with a bad IDB to be read. On a write command, when a bad IDB is sensed, tape position lost will occur. NOTE: If you append to a tape with a bad IDB, you will not receive any DCK error until a write.
02	NOI	6	Noise Record: This bit is set during a space operation when a burst of flux changes, which do not qualify as a record (but too many to ignore), are detected.
01	LXS	S	Limit Exceeded Statically: This bit is set by tension arms that have actuated their limit switches; it remains set when tension arms are returned to normal position. It can be reset only by loading tape.
00	RIB	2	Reverse Into BOT: This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT.

5.2 PACKET PROCESSING

The packet protocol scheme allows the drive to send a large amount of status and error information to the CPU while taking up only two words of Unibus address space. The packet protocol also prevents the drive from updating the error and status information asynchronously, that is, while the CPU is reading the error and status information.

NOTE

This section is not intended to detail all aspects of packet protocol or packet processing. It is intended to illustrate how these concepts are implemented in the TS11 Subsystem.

To allow the drive to take up only two words of address space, we allow the CPU to define a set of locations in memory. These locations (command buffers) are used to tell the drive what operation to perform. The CPU also defines a set of locations (message buffers) in memory where the drive will put the error and status information. The CPU must give both the command buffer address and message buffer address to the drive. The CPU gives the command buffer address to the drive on every command. (The CPU writes the address of the command packet into the TSDB of the drive.) The CPU gives the message buffer address to the drive every time the CPU does a set characteristics command.

To prevent the drive from updating the message buffer while the CPU is reading the message buffer, we have defined the concept of ownership. Both the command and message buffers can be owned. Each buffer may be owned by the drive or the CPU, but not by both simultaneously. Ownership of a buffer can only be transferred by the current owner.

There are four different combinations that transfer the ownership of the two buffers:

- Command buffer CPU to drive by the CPU
- Command buffer drive to CPU by the drive
- Message buffer CPU to drive by the CPU
- Message buffer drive to the CPU by the drive.

The CPU transfers ownership of the command buffer to the drive by writing the address of the command packet into the TSDB. This write clears the TSSR subsystem ready (SSR) bit.

The drive transfers ownership of the command buffer to the CPU by setting the acknowledge (ACK) bit in the message buffer. When the drive outputs the message buffer, the drive sets SSR in the TSSR to indicate that the message is in the message buffer. If the message buffer does not contain the ACK bit, the CPU will know that the drive did not see the last command buffer and the CPU still owns the command buffer. The command may be reissued by the CPU.

The CPU transfers ownership of the message buffer to the drive by setting the ACK bit in the command buffer. If the command buffer does not contain the ACK bit, the drive will know that the CPU did not see the last message buffer and the drive still owns the message buffer. The drive outputs the TSSR again (with the SSR bit up) and interrupts (if IE is set) without sending out a message.

The drive transfers ownership of the message buffer to the CPU in one of two ways. The first way is used after the end of a command: the drive sets the SSR bit in the TSSR to indicate that the command is done (and interrupts if IE is set). The second way is used during an attention (ATTN). SSR will already be up because an ATTN only happens when the drive is inactive. The drive clears SSR, outputs the message, then sets SSR again and interrupts (if IE set). Note that if the CPU writes the TSDB while the SSR is clear during an ATTN, the register modification refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the drive does not own the command buffer. Note that RMR may set in this way on a bug free system because the CPU happened to try to perform a command at the same time the drive wanted to perform an ATTN. All other settings of the RMR indicate a software bug. (The CPU tried to do a command before the previous command was finished.) If the CPU command was lost because the transport was outputting an ATTN message, VOL CHK and INT ENB are not updated. If the CPU command was rejected (illegal command, etc.), VOL CHK and INT ENB are updated to the start of the rejected command.

When the drive is initialized, the drive updates the TSSR. At this time we define both the command and message buffers as belonging to the CPU. When the CPU wants to do a command (the first one must be a set characteristics to set up the message buffer address), the CPU writes the address of the command buffer into the TSDB of the drive. This command must have the ACK bit set to give ownership of the message buffer to the drive. At this point, the drive owns both the command and message buffers.

The drive will execute the set characteristics command and send out a message to the message buffer address with the ACK bit set; this indicates that the drive has recognized the command and is finished with the command buffer. The drive will then set SSR and interrupt (if IE is set). At this point, the CPU owns both the message and command buffers again.

As you can see, the ownership of both buffers transfers simultaneously from CPU to drive and then from drive to CPU.

Now consider the case where ATTNs are enabled by the proper characteristics mode word and the drive wants to do an ATTN. An ATTN will only occur when the drive is not active. If the CPU owns both the command and message buffers, the drive must queue up the ATTN and not do anything until the CPU releases the message buffer on the next command. So when the CPU executes the next command (with the ACK bit set), the drive will output the ATTN message with the ACK bit 0; this indicates that the command was lost (except for the transfer of the message buffer ownership to the drive). The drive refuses to accept ownership of the command buffer. The CPU will then still own the command buffer (because the drive did not accept the command) and will also own the message buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set).

Now consider the case where the CPU wants to be notified of a change in status right away while the drive is inactive for a long period of time. To accomplish this, the drive must own the message buffer for that long period of time. Everything up to now has indicated that the drive gives up the message buffer at the end of every command. The message buffer release command is a special command from the CPU. It tells the drive not to give ownership of the message buffer back to the CPU at the end of the command. The drive does not output a message at the end of the command but just outputs the TSSR (with the SSR bit set) and interrupts (if the proper characteristics mode word is set up). The drive then maintains ownership of the message buffer until an ATTN condition is seen. The drive then immediately clears SSR, outputs the message (with the ACK bit not set since the drive is not responding to a command), and then sets SSR and interrupts (if IE is set). At that time the system is back to the state of the CPU owning both buffers. Another ATTN will not be done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

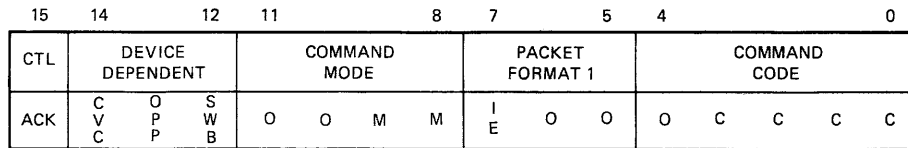
Suppose the CPU has done a message buffer release command and wants to do another command but has not received an ATTN from the drive (so that the drive still owns the message buffer from the message buffer release command). The CPU can do a command without the ACK bit set in the command buffer. At the time of the command, the CPU does not own the message buffer so the CPU cannot release the message buffer. If the CPU does set the ACK bit, nothing will happen (except the CPU might miss an ATTN if the drive was sending out an ATTN at the same time that the CPU was doing a command).

Message packet protocol may be violated if the transport gets an error (NXM, memory parity, serial bus parity error, or I/O silo parity error) during the reading in of the message packet. When one of these errors occurs, the transport always sends out a failure message (because the packet is not reliable).

The system software should be written so it will not crash if the TS11 M7982 interrupts while the CPU is servicing a TS11 M7982 interrupt. However, this case may happen but only if the TS11 should receive a fatal hardware error.

5.2.1 Command Packet/Header Word

The command packet header word is illustrated in Figure 5-5 and defined in Table 5-9. The command code and mode field definitions are given in Table 5-10.



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Figure 5-5 Command Packet Header Word

Table 5-9 Command Packet Header Word Bit Definitions

Bit	Name	Function												
15	Acknowledge	This bit is set when a command is issued and the CPU owns the message buffer. It informs the M7982 that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the transport.												
14-12	Device Dependent Bits/Field	The following shows how these three bits are implemented. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>14</td> <td>CVC</td> <td>Clear volume check</td> </tr> <tr> <td>13</td> <td>OPP</td> <td>Opposite (reverse the execution sequence of the reread commands)</td> </tr> <tr> <td>12</td> <td>SWB</td> <td>Swap bytes</td> </tr> </tbody> </table>	Bit	Name	Definition	14	CVC	Clear volume check	13	OPP	Opposite (reverse the execution sequence of the reread commands)	12	SWB	Swap bytes
Bit	Name	Definition												
14	CVC	Clear volume check												
13	OPP	Opposite (reverse the execution sequence of the reread commands)												
12	SWB	Swap bytes												
11-8	Command Mode Field	This bit acts as an extension to the command code and mode field and allows specification of extended device commands (seek, rewind, erase, write tape mark, etc.). Command code and mode field are detailed in table 5-10.												
7-5	Packet Format #1 Field	The following two values are defined in this field. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit Values</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>One word header; interrupt disable</td> </tr> <tr> <td>100</td> <td>One word header; interrupt enable</td> </tr> </tbody> </table>	Bit Values	Definition	000	One word header; interrupt disable	100	One word header; interrupt enable						
Bit Values	Definition													
000	One word header; interrupt disable													
100	One word header; interrupt enable													
4-0	Command Code	Refer to Table 5-10.												

Table 5-10 Command Code and Mode Field Definitions

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read two)
		0011	Reread next (space forward, read reverse)
00100	Write Characteristics	0000	Load message buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (space reverse, erase, write data)
00110	Write Subsystem Memory	0000	Normal (diagnostic use only)

Table 5-10 Command Code and Mode Field Definitions (Cont)

Command Code Field	Command Name	Command Mode Field	Mode Name
01000	Position	0000	Space records forward
		0001	Space records reverse
		0010	Skip tape marks forward
		0011	Skip tape marks reverse
		0100	Rewind
01001	Format	0000	Write tape mark
		0001	Erase
		0010	Write tape mark entry (space reverse, erase, write tape mark)
01010	Control	0000	Message buffer release
		0001	Rewind and unload
		0010	Clean
01011	Initialize	0000	Drive initialize
01111	Get Status Immediate	0000	Get status (END message only)

Bits 3 and 4 of the command code field determine the format and length of command packets. The command packet formats and lengths are as follows.

Code Bits	Definition
00XXX	Four words (header, two word address, count)
01XXX (header)	Two words (header, parameter word) or one word

The swap byte bit in the command packet header word (bit 12) instructs the M7982 to alter the sequence of storing and retrieving bytes from the CPU's memory. When swap bytes = 1, an industry compatible sequence (beginning with an even byte) is used. When swap bytes = 0, the swapping begins with an odd byte. (This is so only for data transferring; it is ignored otherwise.)

The following figures (Figures 5-6 and 5-7) indicate the memory positions for the bytes as they are read from or written on the tape. In these examples, the bytes of data in the record block on tape are numbered starting at 0. Byte 0 is always the data byte at the beginning of the block (that is, the part of the block that is closest to BOT).

NOTE

When reading in reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

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Figure 5-6 Byte Swap Sequence,
 Forward Tape Direction (Read or Write)

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	1	0
1002	3	2
1004	5	4
1006		6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6

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Figure 5-7 Byte Swap Sequence, Reverse Tape Direction (Read)

5.2.2 Command Packet Examples

Examples of the command packets and operational programming notes used in the TS11 Subsystem are provided in this section. Refer to the figure and section number corresponding to the command packet example you are interested in.

NOTE

All four words of the command packet are always read in, even if the command takes only one word (rewind) or two words (space). Thus, the command packet must contain four words, and it must have good parity because the transport will reject the command packet on the basis of errors in the unused words.

Command Packet Example	Figure Number	Section Number
Get status	5-8	5.2.2.1
Read	5-9	5.2.2.2
Write characteristics	5-10	5.2.2.3
Write	5-11	5.2.2.4
Position	5-12	5.2.2.5
Format	5-13	5.2.2.6
Control	5-14	5.2.2.7
Initialize	5-15	5.2.2.8

5.2.2.1 Get Status Command – Figure 5-8 illustrates the get status command packet. This command causes an update of the five extended status registers in the message buffer area. However, after the end of any command, the TS11 hardware automatically updates the extended status registers. Therefore, this command need only be used when the TS11 has been left idle for some time or when a status register update is desired without performing a read, write, or position tape command.

15	14	12	11	8	7	5	4	0
CTL	DEV.	DEP.	MODE			FMT 1		COMMAND
A C K	C V C	0 0	0	0	0	0	I E 0 0	0 1 1 1 1
NOT USED								

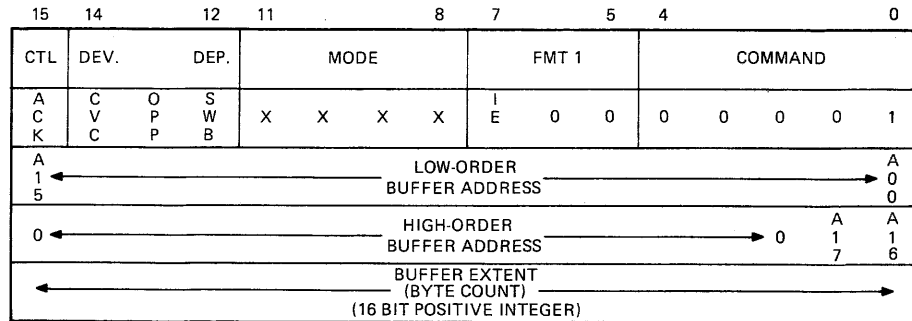
MODE: 0000 = GET STATUS (END MESSAGE ONLY)

NOTE:
SEE MESSAGE PACKET
EXAMPLES FOR DATA FORMAT.

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Figure 5-8 Get Status Command Packet Example

5.2.2.2 Read Command – The read command packet is illustrated in Figure 5-9. There are four modes of operation: read forward, read reverse, reread previous, and reread next. In all cases a read operation is assumed to be for a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, record length short (RLS) will set and a tape status alert (TSA) termination occurs. If the



MODE: 0000 = READ NEXT (FORWARD)
 0001 = READ PREVIOUS (REVERSE)
 0010 = REREAD PREVIOUS (SPACE REV, READ FWD)
 0011 = REREAD NEXT (SPACE FWD, READ REV)

NOTE:
 THE OPPOSITE BIT (OPP) ALTERS THE EXECUTION SEQUENCE OF THE REREAD COMMAND MODES, i.e., SPACE FWD, READ REV BECOMES READ FWD, SPACE REV; SPACE REVERSE, READ FORWARD BECOMES READ REVERSE, SPACE FORWARD.

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Figure 5-9 Read Command Packet Example

record is larger than the byte count, record length long (RLL) and tape status alert (TSA) will be set. Also, any read operation that encounters a tape mark does not transfer any data. In this case tape mark (TMK) and record length short (RLS) are set and a tape status alert (TSA) termination occurs.

Read reverse operations which run into BOT cause Reverse Into BOT (RIB) to set and cause a tape status alert (TSA) termination. Tape motion will stop at BOT. Read reverse while at BOT will cause a function reject (NEF) status, with no tape motion.

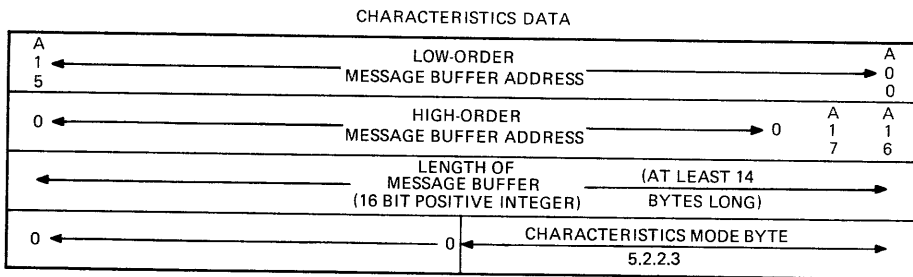
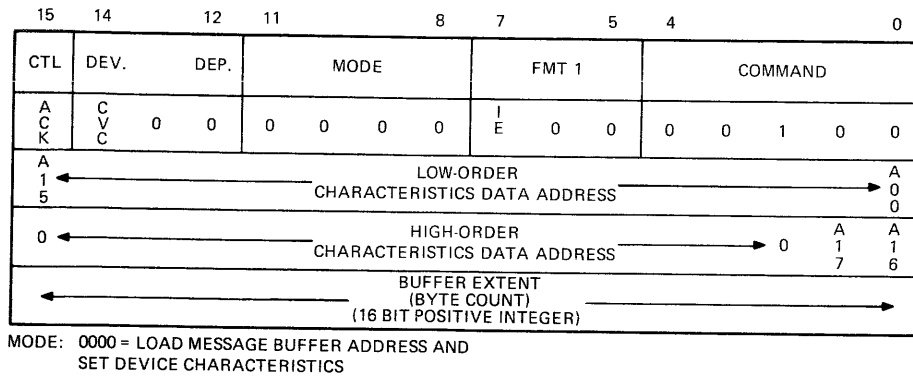
NOTE

When reading reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

5.2.2.3 Write Characteristics Command – Figure 5-10 illustrates the write characteristics command packet. Its objective is to inform the TS11 Subsystem of the location and size of the message buffer in CPU memory space. The message buffer must be at least seven contiguous words long and begin on a word boundary.

The write characteristics command also transfers a characteristics mode word to the transport. This word causes specific actions for certain operational modes. The bits for this word are defined in Table 5-11.

If a good message buffer address has not been loaded with a write characteristics command, the need buffer address (NBA) bit in the TSSR register will be set.



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Figure 5-10 Write Characteristics Command Packet Example

Table 5-11 Write Characteristics Data Bit Definitions

Bit	Name	Definition
15-08	-	Not used.
07	ESS	Enable Skip Tape Marks Stop: When this bit is set, it instructs the transport to stop during a skip tape mark command when a double tape mark (two contiguous tape marks) has been detected. In the default setting of 0, the skip tape marks command will terminate only on tape mark count exhausted or if it runs into BOT.
06	ENB	This bit is only meaningful if the ESS bit is set. If the drive is at BOT, when a skip tape marks command is issued and the first record seen is a tape mark, then the transport will set LET and stop after the first tape mark. If the bit is clear, the drive would not set LET but just count the tape mark and continue.
05	EAI	Enable Attention Interrupts: When this bit is a 0, attention conditions, such as off-line, on-line, and microdiagnostic failure, will not result in interrupts to the CPU. If set to a 1, interrupts will be generated.
NOTE: Transport must own the message buffer, via message buffer release, to set attention interrupts.		
04	ERI	Enable Message Buffer Release Interrupts: If this bit is 0, interrupts will not be generated when a message buffer release command is received by the transport. Upon recognition of the command, only subsystem ready (SSR) will be reasserted. If ERI is a 1, an interrupt will be generated.
03	-	Not used.
02	-	Not used.
01	-	Not used.
00	-	Not used.

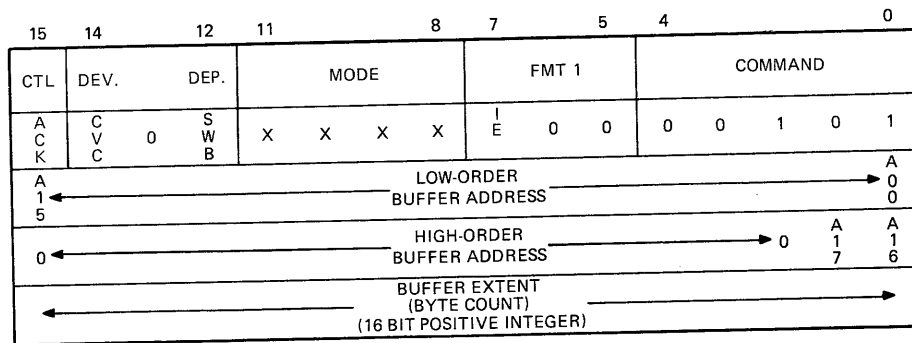
The following notes concern bit usage in the characteristics word.

Interrupts Enabled – If interrupts are enabled (IE), interrupts may occur at any time. This is due to the possibility of diagnostic interrupts, ACLO, or CROM parity errors occurring immediately after normal terminations (even if ATTN interrupts are not enabled). The software must therefore defend against unexpected interrupts. The drive may not be usable, but the software still should not crash.

Attention Interrupts Enabled – With attention interrupts enabled, a nonfatal diagnostic failure will not be reported until control of the message buffer is returned to the transport. A fatal failure may interrupt at any time as long as interrupt enable is set. It should also be noted that the drive could break in such a way that interrupts may be issued even with IE reset.

Attention Interrupts Disabled – With attention interrupts disabled, a diagnostic failure will not be noticeable until the next command is issued. At this time the command will be rejected.

5.2.2.4 Write Command – Figure 5-11 illustrates the write command packet. There are two modes: write data and write data retry (space, reverse, erase, write data). Each operation is straightforward and designed to transfer data onto tape in the forward direction only.



MODE: 0000 = WRITE DATA
 0010 = WRITE DATA RETRY (SPACE REV,
 ERASE, WRITE DATA)

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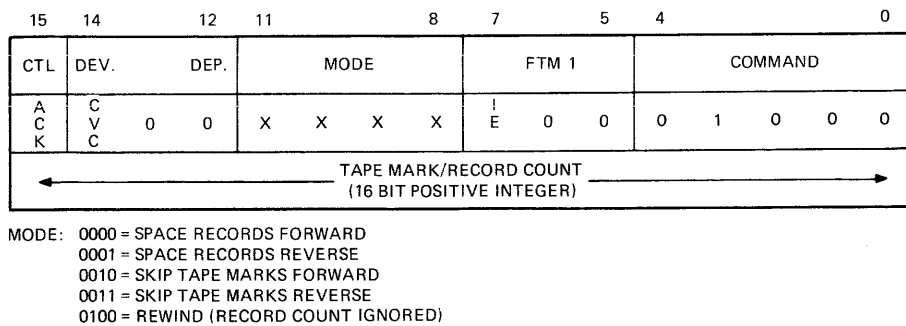
Figure 5-11 Write Command Packet Example

If a write command is executed at or beyond the EOT marker a tape status alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction or a subsystem initialize.

If a write command is executed anywhere and the identification burst (IDB) was previously written bad or was not found when it left BOT, then density check (DCK) is set and tape position lost termination occurs.

5.2.2.5 Position Command – Figure 5-12 illustrates the position command packet. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, and to rewind to BOT. An exact tape mark/record count must be the second word of the packet for skip tape mark and space record commands.

A space records operation automatically terminates when a tape mark is traversed. Also, record length short (RLS) is set if the record count was not decremented to zero.



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Figure 5-12 Position Command Packet Example

A skip tape marks command terminates when it encounters a double tape mark and the enable skip stop mode is specified (ESS bit set) in the characteristics word. Termination will also occur if a tape mark is the first record off BOT and ESS and ENB bits are set in the characteristics word. Record length short (RLS) is set if the record count is not decremented to zero.

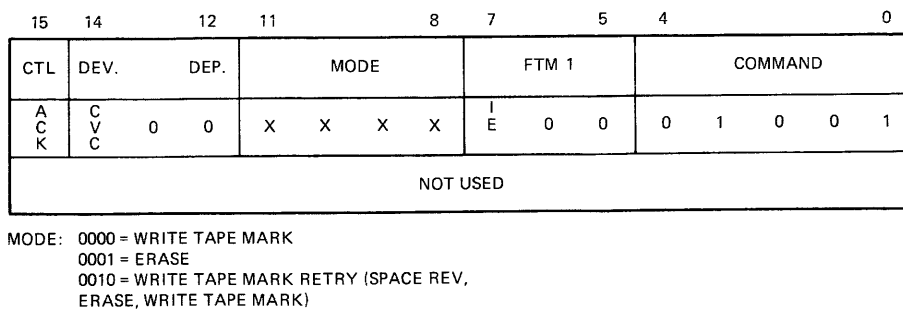
A space records reverse or skip tape marks reverse, which runs into BOT, sets reverse into BOT (RIB) and causes a tape status alert termination.

When a rewind command is issued, the interrupt will not occur until the tape reaches BOT in the forward direction and has begun to decelerate. Due to tape speed during rewind, the drive overshoots BOT in the reverse direction and then moves the tape forward until BOT is located before terminating the operation. Normal termination will be indicated if the operation is completed without incident. If the tape is already at BOT, the rewind will still be done to make sure the tape is positioned properly.

NOTE

If the tape is positioned between BOT and the first record and you do a space reverse or skip reverse, RIB will set and the residual frame count equals the specified count in the original command.

5.2.2.6 Format Command – Figure 5-13 illustrates the format command packet. This command can write a tape mark, rewrite a tape mark, and erase tape. In all cases, executing a format command at or beyond EOT will cause a tape status alert (TSA) termination. The EOT bit will remain set until passed in the reverse direction. A subsystem initialize can also reset the EOT bit. Also, any format command executed with density check (DCK) set will cause a tape position lost termination.



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Figure 5-13 Format Command Packet Example

Density check is set when an invalid identification burst (IDB) is read off BOT. This occurs in a read after write mode within the first three inches of tape and is transparent to the user's operation.

The erase command will cause three inches of tape to be erased. This length is controlled automatically by the transport hardware. Successive erase commands can be used to erase more than three inches (in three inch increments).

5.2.2.7 Control Command – Figure 5-14 illustrates the control command packet. The three modes of operation are message buffer release, unload, and clean. The message buffer release command, when executed with the ACK bit set, allows the transport to own the message buffer so it can update the status in the message buffer area on an ATTN. This is beneficial when the operating system is processing data in other areas not concerned with operating the TS11 Subsystem and the host wants to know the current drive status.

15	14	12	11	8	7	5	4	0			
CTL	DEV.	DEP.	MODE				FMT 1		COMMAND		
A C K	C V C	0 0	X	X	X	X	I E	0 0	0 1	0 1	0 0
NOT USED											

MODE: 0000 = MESSAGE BUFFER RELEASE
 0001 = UNLOAD
 0010 = CLEAN TAPE

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Figure 5-14 Control Command Packet Example

The unload command is designed to rewind tape completely onto the supply reel. When the command is executed, termination occurs immediately; an interrupt will occur if IE is set.

The clean tape command moves ten inches of tape over the tape cleaners and returns it to the original position. Successive clean tape commands are not recommended since the tape may creep outside the interrecord gap (IRG) margins. Also, the clean tape command does not recognize BOT. (That is, you can clean tape and reverse past BOT and back again without setting status bits.)

5.2.2.8 Initialize Command – Figure 5-15 illustrates the initialize command packet. This command is not very useful, but is included for compatibility with packet protocol. A drive initialize can be done by a write to the TSSR, as this action does not need a command packet.

15	14	12	11	8	7	5	4	0			
CTL	DEV.	DEP.	MODE				FMT 1		COMMAND		
A C K	C V C	0 0	0	0	0	0	I E	0 0	0 1	0 1	1 1
NOT USED											

MODE: 0000 = DRIVE INITIALIZE

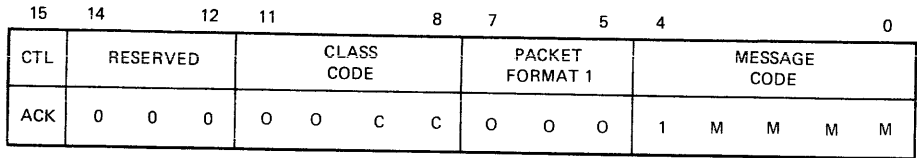
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Figure 5-15 Initialize Command Packet Example

The drive initialize command is a no-op. It results in a message update, just like a get status, if there are no microdiagnostic or runaway errors. However, if errors are displayed, the command does the same thing as a write to the TSSR. Section 5.1.3 contains TSSR details.

5.2.3 Message Packet-Header Word

The first message packet header word is illustrated in Figure 5-16 and defined in Table 5-12.



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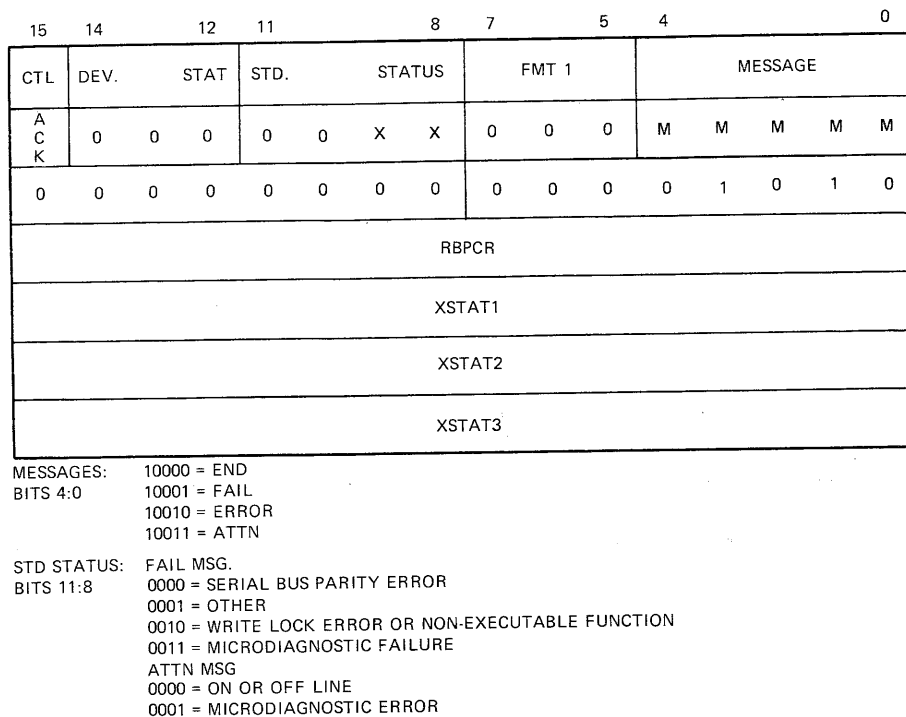
Figure 5-16 Message Packet First Header Word

Table 5-12 Message Packet First Header Word Bit Definitions

Bit	Name	Function																					
15	Acknowledge	This bit is used by the M7982 to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the drive does not own the command buffer.																					
14-12	Reserved	These bits are reserved for future expansion.																					
11-8	Class Code Field	These bits define the class of failures found in the rest of the message buffer.																					
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>MSG Type</th> <th>Class Value</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>ATTN</td> <td>0000</td> <td>On- or off-line</td> </tr> <tr> <td>ATTN</td> <td>0001</td> <td>Microdiagnostic failure</td> </tr> <tr> <td>FAIL</td> <td>0000</td> <td>Serial bus parity error (packet bad)</td> </tr> <tr> <td>FAIL</td> <td>0001</td> <td>Other (ILC, ILA, NBA)</td> </tr> <tr> <td>FAIL</td> <td>0010</td> <td>Write lock error or non-executable function</td> </tr> <tr> <td>FAIL</td> <td>0011</td> <td>Microdiagnostic error</td> </tr> </tbody> </table>	MSG Type	Class Value	Definition	ATTN	0000	On- or off-line	ATTN	0001	Microdiagnostic failure	FAIL	0000	Serial bus parity error (packet bad)	FAIL	0001	Other (ILC, ILA, NBA)	FAIL	0010	Write lock error or non-executable function	FAIL	0011	Microdiagnostic error
MSG Type	Class Value	Definition																					
ATTN	0000	On- or off-line																					
ATTN	0001	Microdiagnostic failure																					
FAIL	0000	Serial bus parity error (packet bad)																					
FAIL	0001	Other (ILC, ILA, NBA)																					
FAIL	0010	Write lock error or non-executable function																					
FAIL	0011	Microdiagnostic error																					
7-5	Packet Format #1 Field	The single value supported by the TS11 is as follows.																					
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>One word header</td> </tr> </tbody> </table>	Value	Definition	000	One word header																	
Value	Definition																						
000	One word header																						
4-0	Message Code																						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Term Class</th> <th>Value</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0,2</td> <td>10000</td> <td>End</td> </tr> <tr> <td>3</td> <td>10001</td> <td>Fail</td> </tr> <tr> <td>4,5,6,7</td> <td>10010</td> <td>Error</td> </tr> <tr> <td>1,7</td> <td>10011</td> <td>Attention</td> </tr> </tbody> </table>	Term Class	Value	Definition	0,2	10000	End	3	10001	Fail	4,5,6,7	10010	Error	1,7	10011	Attention						
Term Class	Value	Definition																					
0,2	10000	End																					
3	10001	Fail																					
4,5,6,7	10010	Error																					
1,7	10011	Attention																					

5.2.4 Message Packet Example

All message packets are identical. Each message packet contains the message packet header word just described, plus a data length field word and the five extended status registers. Figure 5-17 illustrates the message packet format.



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Figure 5-17 Message Packet Example

5.3 OPERATIONAL INFORMATION

The following information considers the operation and programming requirements of the TS11 Sub-system.

5.3.1 Unibus Registers

Each TS11 has two Unibus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a sub-system initialize command, and reading the TSSR reads device status.

The TSDB register is the only register written to during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the drive's Unibus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words in the command packet. The words of the command packet tell the transport the function to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

5.3.2 Command and Message Packets

Command packets must reside on modulo — 4 address boundaries within CPU memory space. This means the starting address of the packet must be divisible by 4 (that is, octal 00, 04, 10, 14, etc.).

All four words of a command packet must exist and have good memory parity, even if all four words are not used by a command. (For instance, rewind uses only one word.)

Message packets are issued by the subsystem and are deposited into the CPU's memory space. Controlled operation of the TS11 requires that it be supplied a message buffer address on a write characteristics command. The five extended status registers are stored in this message buffer area. The END message packet, which results at the end of any command, contains these extended status words.

5.3.3 Special Conditions and Errors

Table 5-13 includes the meanings of the binary values within the termination class code field in the TSSR register. Table 5-14 shows the fatal class code field for the TSSR.

Table 5-13 Termination Class Codes

TC2-0 Value	Msg Type	Offset	Meaning
0	END	00	Normal Termination: This bit indicates the operation was completed without incident.
1	ATTN	02	Attention Condition: This code indicates that the transport has undergone a status change: going off-line, coming on-line, or a microdiagnostic failure.
2	END	04	Tape Status Alert: This bit indicates a status condition has been encountered that may have significance to the program. Bits of interest include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject: This bit indicates the specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC and ILA.
4	ERR	10	Recoverable Error: This bit indicates tape position is one record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	ERR	12	Recoverable Error: This bit indicates tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.
6	ERR	14	Unrecoverable Error: This bit indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ ERR	16	Fatal Subsystem Error: This bit indicates the subsystem is incapable of properly performing commands or at least that the subsystem's integrity is seriously questionable. Refer to the fatal class code field in the TSSR register for additional information on the type of fatal error.*

* The fatal class code field in the TSSR register is defined in Table 5-14. The meanings are valid when the termination class code bits are all set (value of 7, offset of 16).

Table 5-14 TSSR Fatal Class Codes

FC1-0 Value	Meaning
0	This bit indicates there is an internal microdiagnostic failure in the diagnostic mode or a capstan runaway in the operational mode (337 octal in operator panel). See the fatal error code byte (XSTAT3) for the diagnostic function. This is cleared by the drive initialize command or subsystem initialize. Subsequent tape operations will not be accepted (command reject) until, as a minimum, a drive initialize is issued.
1	There is a I/O CROM parity error. This is cleared by drive initialize or subsystem initialize.
2	There is a microprocessor CROM, I/O silo, serial bus parity error, or another fatal error. This is cleared only by subsystem initialize.
3	Loss of ac power has been detected and a power down is in effect. This is cleared only by subsystem initialize.

5.3.4 Status Error Handling Notes

TSSR error bits, other than the fatal class, termination class, and SC bits, are cleared by loading a command pointer into the TSDB register. SC is reset if it is due to a TSSR error (UPE, SPE, RMR, or NXM). Extended status error bits are cleared after the END message is sent.

All commands (even get status command) clear the XSTAT error bits; except XSTAT3 bits 15 through 8 (microdiagnostic error code) and bit LXS are not cleared.

If a density check condition is detected during a read, space, or skip function, the DCK bit is set, but the operation is not stopped. If DCK is the only status bit set during the operation, normal termination is reported. This allows tapes with good data but bad density check areas to be read. If a wrong density tape has been mounted, other errors will be reported and the operation will stop. Note that if only the density check area is bad, the density check indicator on the drive's operator panel lights, even though the data records might be the correct density. The DCK indicator will remain lit until BOT is encountered again or until a subsystem initialize is performed. Note that if you begin reading a tape, get a density check condition with no other errors, then append to the tape; the write will get a termination class code of 6. This indicates that the tape position is lost because density check will remain set. The whole tape should be copied over so that drives depending on the IDB will be able to read the tape.

A command is not responded to while another command is in progress (result is RMR), except in the following cases.

1. A DATO (word access) to the TSSR (subsystem initialize) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the subsystem's memory (VCK reset, EOT, etc.) are erased. Also, if the on-line switch is on, the drive performs an auto-load sequence and positions the tape at BOT.
2. The transport responds to any nontape motion command while performing a rewind unload (while the drive is off-line) because SSR is still up.

The transport also responds to any nontape motion commands (get status, drive initialize, set characteristics, and message buffer release) when off-line, except when in maintenance mode. (The subsystem ready command, SSR, is not asserted in this case and results in RMR.)

The following failures can occur without resulting in an interrupt, even though the specified command had interrupt enable set.

- SPE The possibility exists that the drive cannot transfer valid data or command information via the serial bus to the TS11. In this case the SC, TC2, TC1, and TC0 bits are not valid either.
- NXM They might occur before the interrupt enable bit is fetched as part of the command
- UPE packet.
- BPE

These cases may result in a hung controller (SSR does not come up again until a subsystem initialize). The same is true when the fatal class codes are 2 or 3.

5.4 OPERATIONAL DIFFERENCES

The following describes three differences in the operation of the TS11 Subsystem compared to earlier DECmagtape products.

- The skip tape marks (files) function is implemented in the hardware on this subsystem. Earlier DECmagtapes had this function emulated by the software driver through use of the space records command.
- If a space records command is issued while positioned at or beyond EOT, the operation is not terminated after one record has been traversed. The termination criteria remains the same as for any other location on tape; that is, record count exhausted or tape mark encountered. The skip tape marks command operates in the same manner. EOT is not allowed to alter its operation.
- A skip files command could take 15 to 20 minutes to complete to the end of a 2,400 foot reel of tape. There is no abort procedure other than a subsystem initialize. This will cause an automatic load sequence.

PROGRAMMER'S NOTE

As a debugging aid, set the message buffer to all 1s (ones). This eliminates any confusion that might be caused by earlier messages.

